GT93C76

Microwire

8K Bits

Serial EEPROM

Table of Contents

GT93C76

1. Features

- Standard Microwire Interface
- Wide-voltage Operation
  - V_{CC} = 1.8V to 5.5V
- Speed
  - 1 MHz (1.8V), 2 MHz (2.5V), 3 MHz (5.5V)
- User Configured Memory Organization
  - 512x16-bit (ORG = V_{CC} or Floating)
  - or 1024x8-bit (ORG = 0V)
- Self timed write cycle: 5 ms (max.)
- Hardware and software write protection
  - Defaults to write-disabled state at power-up
  - Software instructions for write-enable/disable
- CMOS technology
- Versatile, easy-to-use interface
  - Automatic erase-before-write
  - Programming status indicator
  - Byte, Word and chip single erasable
  - Chip select enables power savings
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 40 years
- Packages: SOIC, TSSOP,UDFN and PDIP
- Lead-free, RoHS, Halogen free, Green

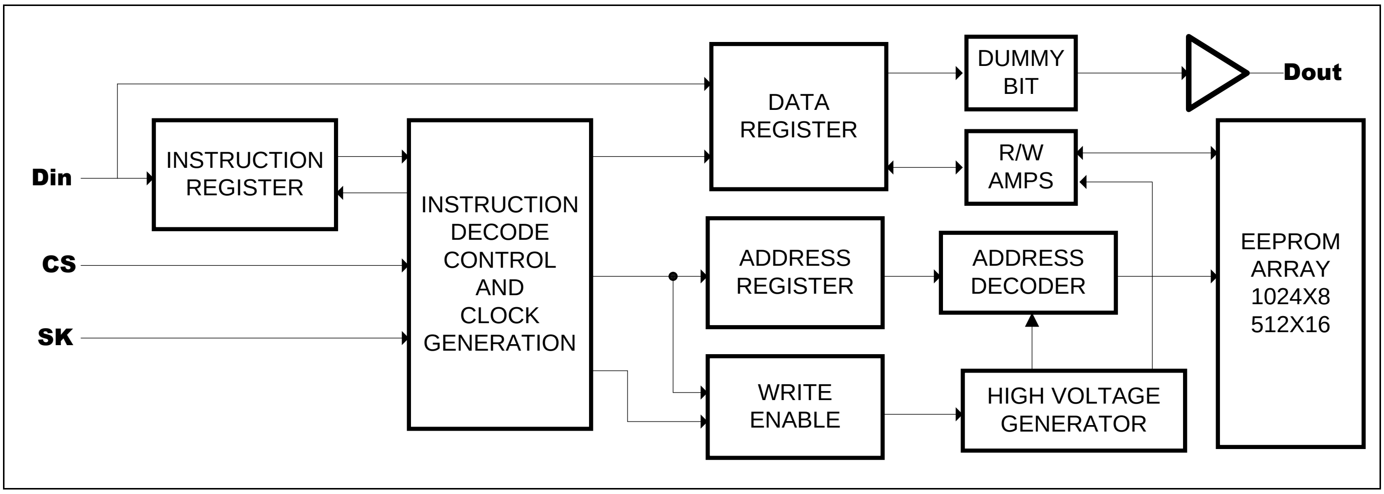
2. General Description

The GT93C76 is 8kb non-volatile serial EEPROM with memory array of 8,192 bits. The array can be organized as either 1024 bytes of 8 bits or 512 words of 16 bits via the ORG control. Utilizing the CMOS design and process, these products provide low standby current and low power operations. The devices can operate in a wide supply voltage range from 1.8V to 5.5V, with frequency up to 3MHz.

When the ORG pin is connected to V_{CC} or floating, x16 is selected. Conversely, when it is connected to ground, x8 is chosen.

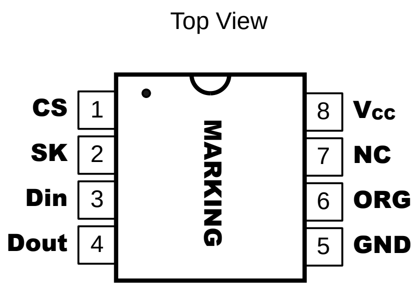
An instruction Op-code defines the various operations of the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all write and erase instructions are merely accepted while the device is in write enable mode. A selected x8 byte or x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the WRITE ALL or ERASE ALL instruction can program or erase the entire array, respectively. Once a device begins its self-timed program procedure, the data out pin (D_{OUT}) can indicate the READY/BUSY status by raising chip select (CS). The devices can output any number of consecutive bytes/words using a single READ instruction.

3. Functional Block Diagram



4. Pin Configuration

4.1 8-Pin SOIC, TSSOP,UDFN and PDIP



4.2 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	CS	I	Chip Select
2	SK	I	Serial Data Clock
3	D_{IN}	I	Serial Data Input
4	D_{OUT}	O	Serial Data Output
5	GND	-	Ground
6	ORG	I	Organization Select
7	NC	-	Not Connect
8	V_{CC}	-	Supply Voltage

5. Device Operation

The GT93C76 is controlled by a set of instructions which are clocked-in serially on the D_{IN} pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the D_{IN} value must be stable at either LOW or HIGH. Each instruction begins with a start bit of the logical "1" or HIGH. Following this are the Op-code, address field, and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

5.1 Read

The READ instruction is the only instruction that outputs serial data on the D_{OUT} pin. After the read instruction and address have been decoded, data is transferred from the selected memory array into a serial shift register. (Please note that one logical "0" bit precedes the actual 8 or 16-bit output data string.) The output on D_{OUT} changes during the low-to-high transitions of SK (see Figure 5.10-2).

The GT93C76 is designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

5.2 Write Enable

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (See Figure 5.10-3) (Note: Chip select must remain LOW until V_{CC} reaches its operational value.)

5.3 Write Disable

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

5.4 Write

The WRITE instruction writes 8 or 16 bits of data into the specified memory location. After the last data bit has been applied to D_{IN}, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN). If CS is brought HIGH, after a minimum wait of 200 ns after the falling edge of CS (T_{CS}) D_{OUT} will indicate the READY/BUSY status of the chip. Logical "0" means programming is still in progress; logical "1" means the selected memory array has been written, and the part is ready for another instruction (see Figure 5.10-4). The READY/BUSY status will not be available if the CS input goes HIGH after the end of the self-timed programming cycle (Twp).

5.5 Write All Memory

The write all (WRALL) instruction programs entire memory with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (T_{CS}), the D_{OUT} pin indicates the READY/BUSY status of the chip (see Figure 5.10-5).

5.6 Erase

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of T_{CS}, will cause D_{OUT} to indicate the READ/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction (see Figure 5.10-7).

5.7 Erase All Memory

Full chip erase (ERAL) is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1" (see Figure 5.10-8). V_{CC} is required to be above 4.5V for ERALL to function properly.

5.8 Power-On Reset

The device incorporates a Power-On Reset (POR) circuitry which protects the internal logic against powering up into a wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This POR feature protects the device being 'brown-out' due to a sudden power loss or power cycling.

In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset (POR) circuit is embedded. During power-up, the device does not respond to any instruction until V_{CC} has reached a minimum stable level above the reset threshold voltage. Once V_{CC} passes the POR threshold, the device is reset and enters in Standby mode. This can also avoid any inadvertent Write operations during power-up stage. During power-down process, the device must enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will enter standby mode after current operation completes, provided that no internal write operation is in progress.

5.9 Instruction Set

Instruction [2]	Start Bit	OP Code	8-bit Organization (ORG = GND)			16-bit Organization (ORG = V_{CC} or Floating)		
			Address[1]	Data[1]	Required Clock Cycles	Address[1]	Data[1]	Required Clock Cycles
WDS (Write Disable)	1	00	00x xxxx xxxx	—	14	00 xxxx xxxx	—	13
WEN (Write Enable)	1	00	11x xxxx xxxx	—	14	11 xxxx xxxx	—	13
ERAL (Erase All Memory)	1	00	10x xxxx xxxx	—	14	10 xxxx xxxx	—	13
WRAL (Write All Memory)	1	00	01x xxxx xxxx	(D_7-D_0)	22	01 xxxx xxxx	(D_{15}-D_0)	29
WRITE	1	01	x(A_9-A_0)	(D_7-D_0)	22	x(A_8-A_0)	(D_{15}-D_0)	29
READ	1	10	x(A_9-A_0)	—		x(A_8-A_0)	—	
ERASE	1	11	x(A_9-A_0)	—	14	x(A_8-A_0)	—	13

Notes: [1] x = Don't care bit.

[2] Exact number of clock cycles is required for each Op-code instruction.

5.10 Diagrams

Figure 5.10-1. Synchronous Data Timing

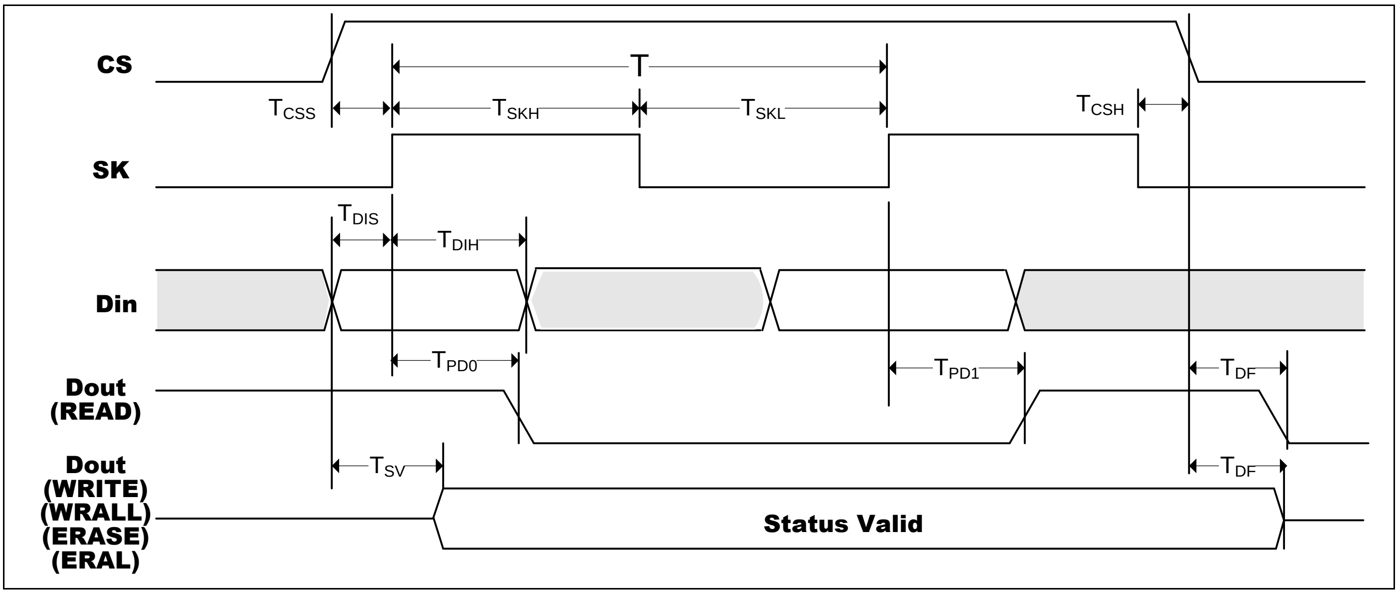
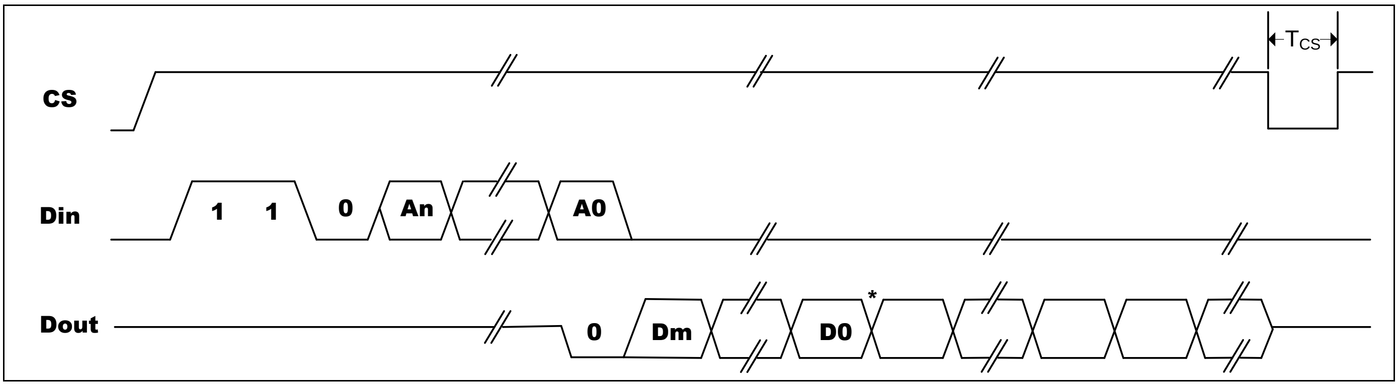


Figure 5.10-2. Read Cycle Timing



Notes: * Address Pointer Cycles to the Next Register

Figure 5.10-3. Write Enable (WEN) Cycle Timing

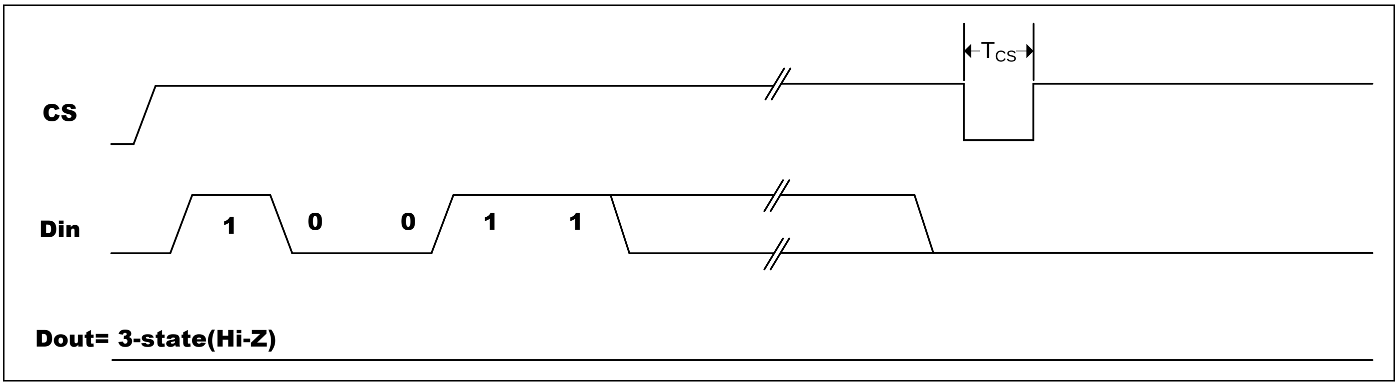
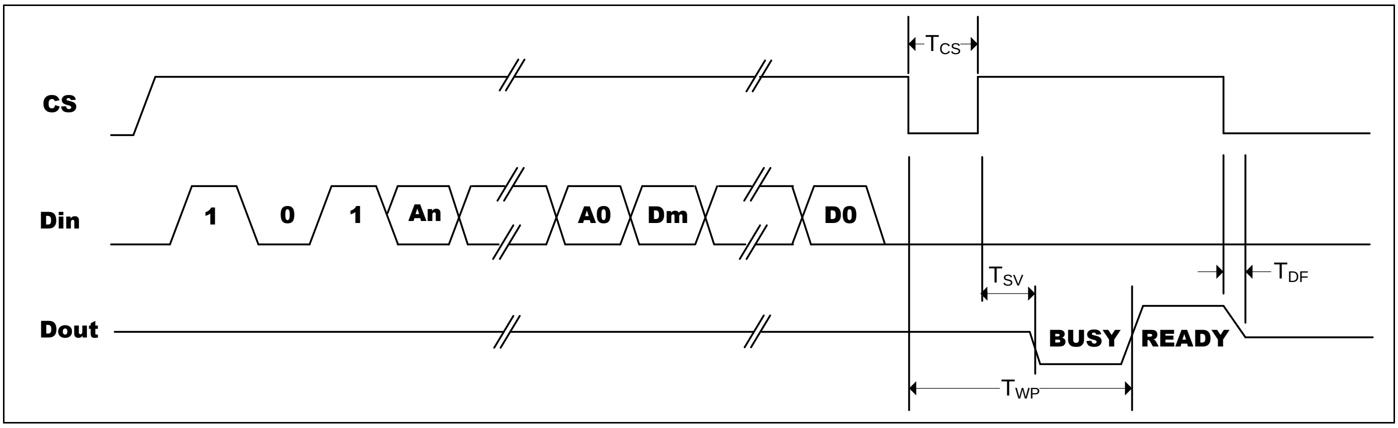
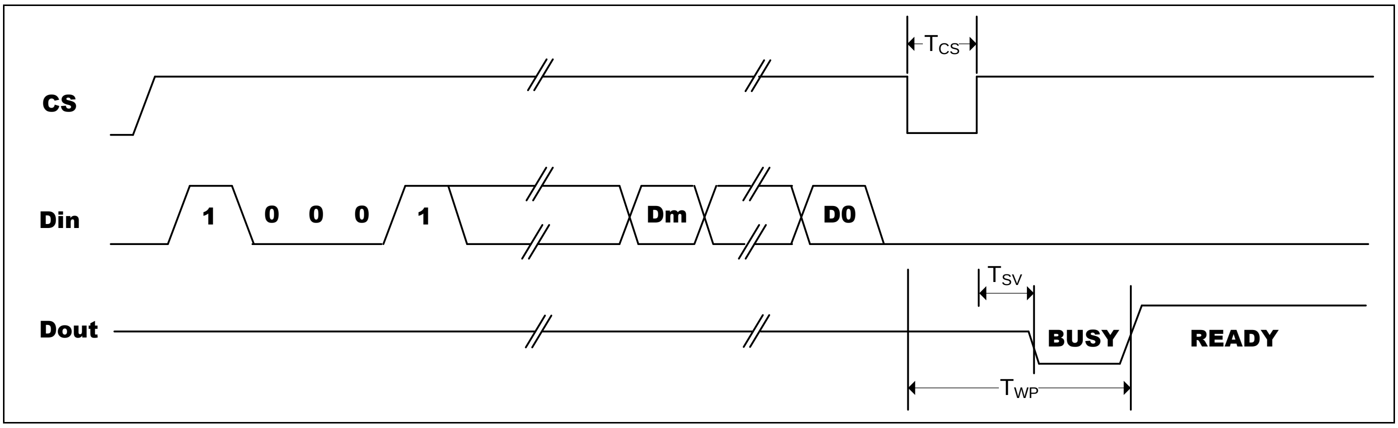


Figure 5.10-4. Write (Write) Cycle Timing



Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.
[2] To determine data bits An - A0 and data bits Dm-D0, see Instruction Set for the appropriate device.

Figure 5.10-5. Write All (WRALL) Cycle Timing



Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.
[2] To determine data bits Dm-D0, see Instruction Set for the appropriate device.

Figure 5.10-6. Write Disable (WDS) Timing

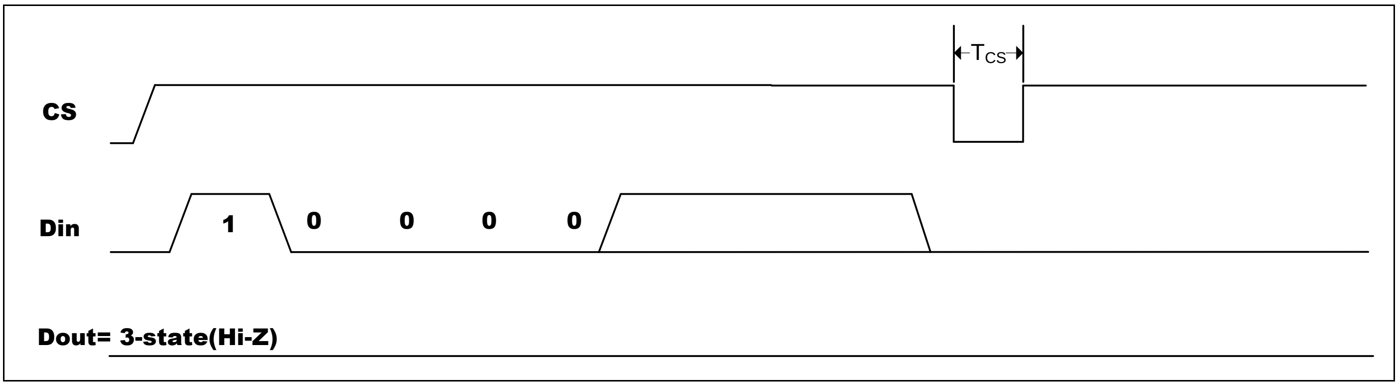
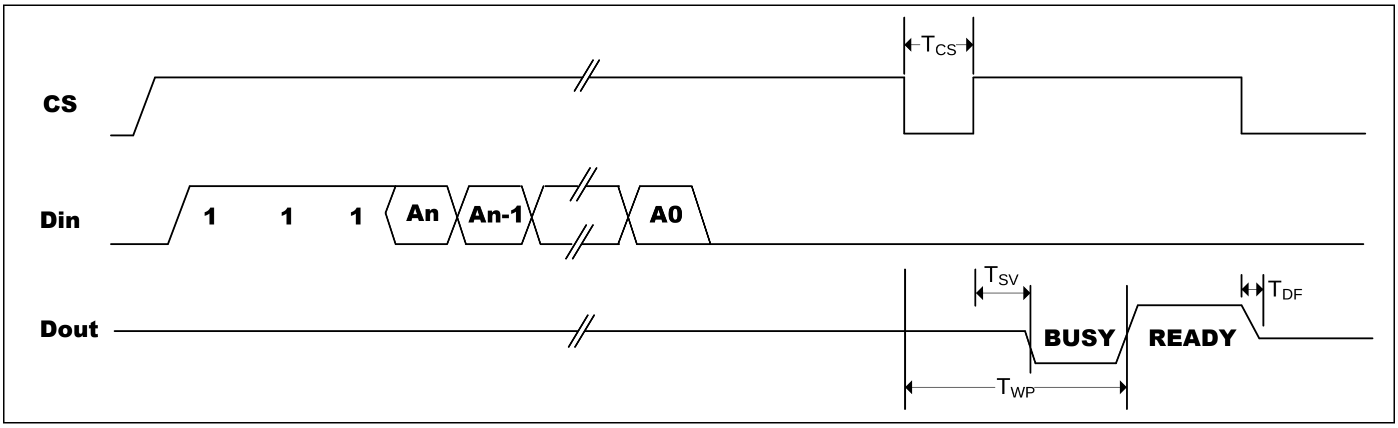


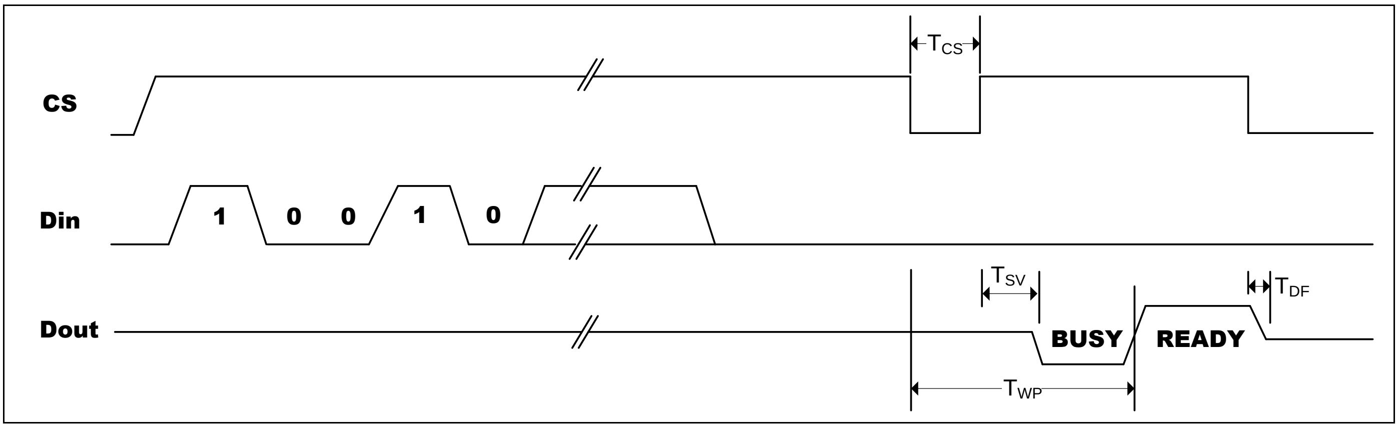
Figure 5.10-7. Erase (Erase) Cycle Timing



Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

[2] To determine data bits An - A0, see Instruction Set for the appropriate device.

Figure 5.10-8. Erase All (ERAL) Cycle Timing



Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

[2] To determine data bits An - A0, see Instruction Set for the appropriate device.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	-0.5 to + 6.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40°C to +85°C	1.8V to 5.5V

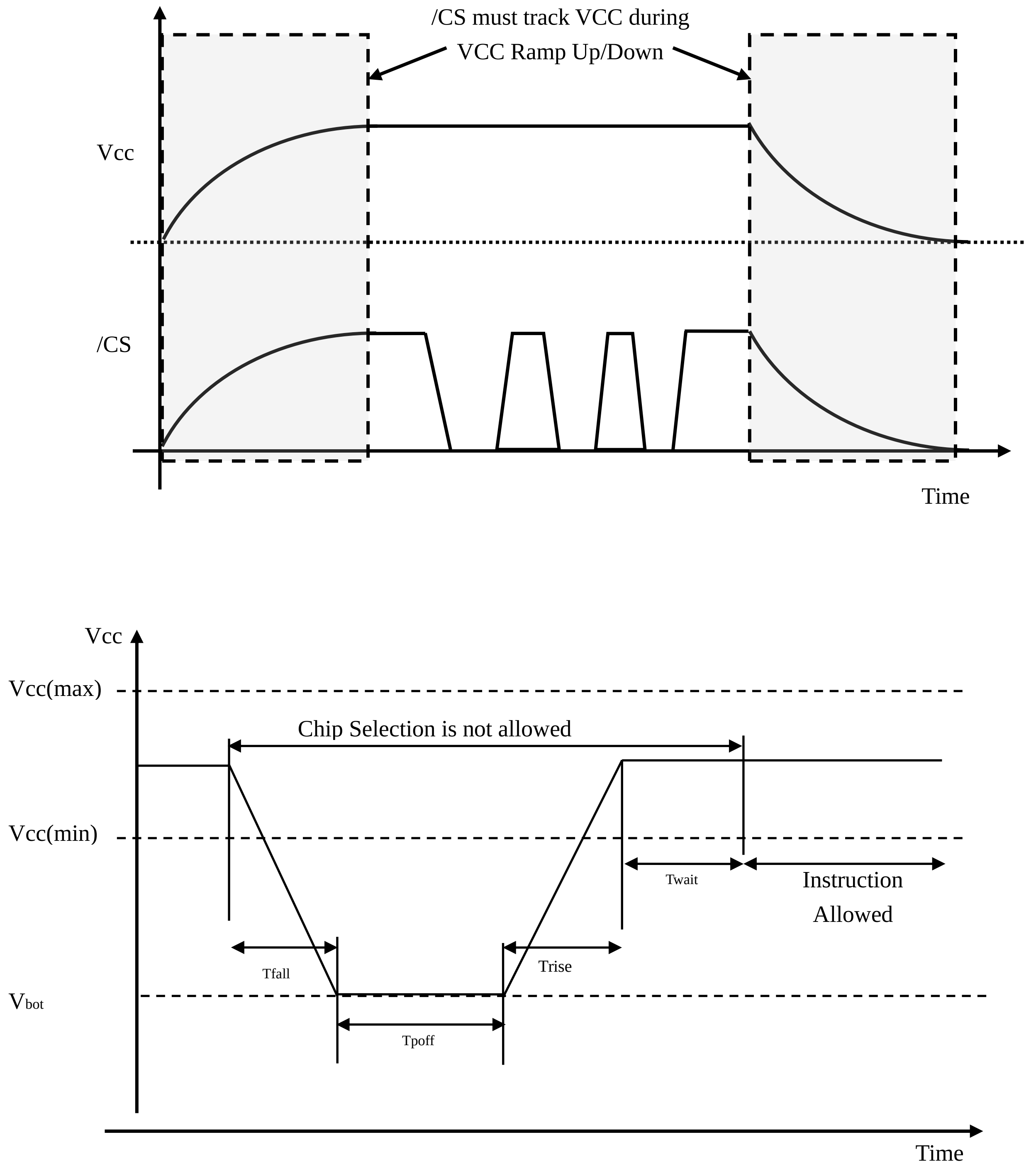
Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

6.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

6.4 Power Up/Down and Voltage Drop



Power down-up Timing

Symbol	Parameter	min	max	unit
V_{bot}	VCC at power off		0.2	V
Tfall	VCC min to Vbot	1		ms
Tpoff	VCC at power off time	100		ms
Trise	Vbot to VCC min		1	ms
Twait	VCC Min to Instruction	500		us

* All parameters may be changed after the design or process change.

6.5 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C

Symbol	Parameter[1]	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		1.8	5.5	V
V_{OL1}	Output LOW Voltage	V_{CC} = 1.8V~2.5V, I_{OL} = 100 uA	—	0.2	V
V_{OL2}	Output LOW Voltage	V_{CC} = 2.5V~5.5V, I_{OL} = 2.1 mA	—	0.4	V
V_{OH1}	Output HIGH Voltage	V_{CC} = 1.8V~2.5V, I_{OH} = -0.1mA	V_{CC} – 0.2	—	V
V_{OH2}	Output HIGH Voltage	V_{CC} = 2.5V~5.5V, I_{OH} = -0.4mA	0.8*V_{CC}	—	V
V_{IH}	Input HIGH Voltage	1.8V to 5.5V	0.7*V_{CC}	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage	1.8V to 5.5V	-0.3	0.2*V_{CC}	V
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC} (CS, SK, D_{IN}, ORG)	0	2.5	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, CS = 0V	0	2.5	μA

Power Supply Characteristics

Industrial: T_A = –40°C to +85°C

Symbol	Parameter [1]	V_{CC}	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			1.8		5.5	V
I_{SB1}	Standby current	1.8	CS = GND, SK = GND, ORG = V_{CC} or Floating (x16), D_{IN} = V_{CC} or GND	—	0.1	1	μA
		2.5		—	0.1	2	μA
		5.5		—	0.2	4	μA
I_{SB2}	Standby current	1.8	CS = GND, SK = GND, ORG = GND (x8), D_{IN} = V_{CC} or GND	—	6	10	μA
		2.5		—	6	10	μA
		5.5		—	10	15	μA
$I_{CC-Read}$	Read current	1.8	CS = V_{IH}, SK = 1 MHz	—	0.1	1	mA
		2.5	CS = V_{IH}, SK = 2 MHz	—	0.2	1	mA
		5.0	CS = V_{IH}, SK = 2 MHz	—	0.5	2	mA
$I_{CC-Write}$	Write current	1.8	CS = V_{IH}, SK = 1 MHz	—	0.5	1	mA
		2.5	CS = V_{IH}, SK = 2 MHz	—	1	2	mA
		5.0	CS = V_{IH}, SK = 2 MHz	—	2	3	mA

6.6 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.8V to 5.5V

Symbol	Parameter [1] [2]	1.8V≤V_{CC}<2.5V		2.5V≤V_{CC}<4.5V		4.5V≤V_{CC}≤5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCK}	SCK Clock Frequency	0	1	0	2	0	3	MHz
T_{SKH}	SK High Time	250	—	200	—	200	—	ns
T_{SKL}	SK Low Time	250	—	200	—	100	—	ns
T_{CS}	Minimum CS LOW Time	250	—	200	—	200	—	ns
T_{CSS}	CS Setup Time	200	—	100	—	50	—	ns
T_{CSH}	CS Hold Time	0	—	0	—	0	—	ns
T_{DIS}	D_{IN} Setup Time	100	—	50	—	50	—	ns
T_{DIH}	D_{IN} Hold Time	50	—	50	—	50	—	ns
T_{PD1}	Output Delay to "1"	—	400	—	200	—	100	ns
T_{PD0}	Output Delay to "0"	—	400	—	200	—	100	ns
T_{SV}	CS to Status Valid	—	400	—	200	—	200	ns
T_{DF}	CS to D_{OUT} in 3-state	—	100	—	100	—	100	ns
T_{WP}	Write Cycle Time	—	10	—	5	—	5	ms

Notes: [1] The parameters are characterized but not 100% tested.
[2] AC measurement conditions:
C_L = 100 pF

7. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

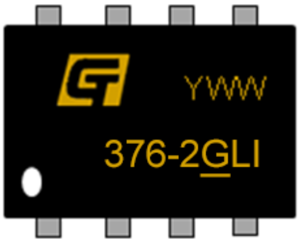
Voltage Range	Part Number*	Package (8-pin)*
1.8V to 5.5V	GT93C76-2GLI-TR	150-mil SOIC
	GT93C76-2ZLI-TR	3 x 4.4 mm TSSOP
	GT93C76-2PLI	300-mil PDIP
	GT93C76-2UDLI-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel “-TR” (4K per reel).
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

8. Top Markings

8.1 SOIC Package

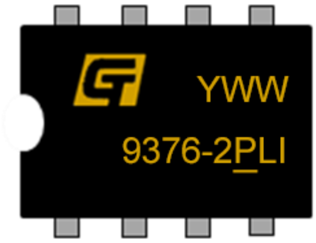


G: Giantec Logo
376-2GLI: Part Number GT93C76-2GLI-TR
YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package

GT: Giantec Logo
376-2ZLI: Part Number, GT93C76-2ZLI-TR
YWW: Date Code, Y=year, WW=week

8.3 PDIP Package



GT: Giantec Logo
9376-2PLI: Part Number GT93C76-2PLI
YWW: Date Code, Y=year, WW=week

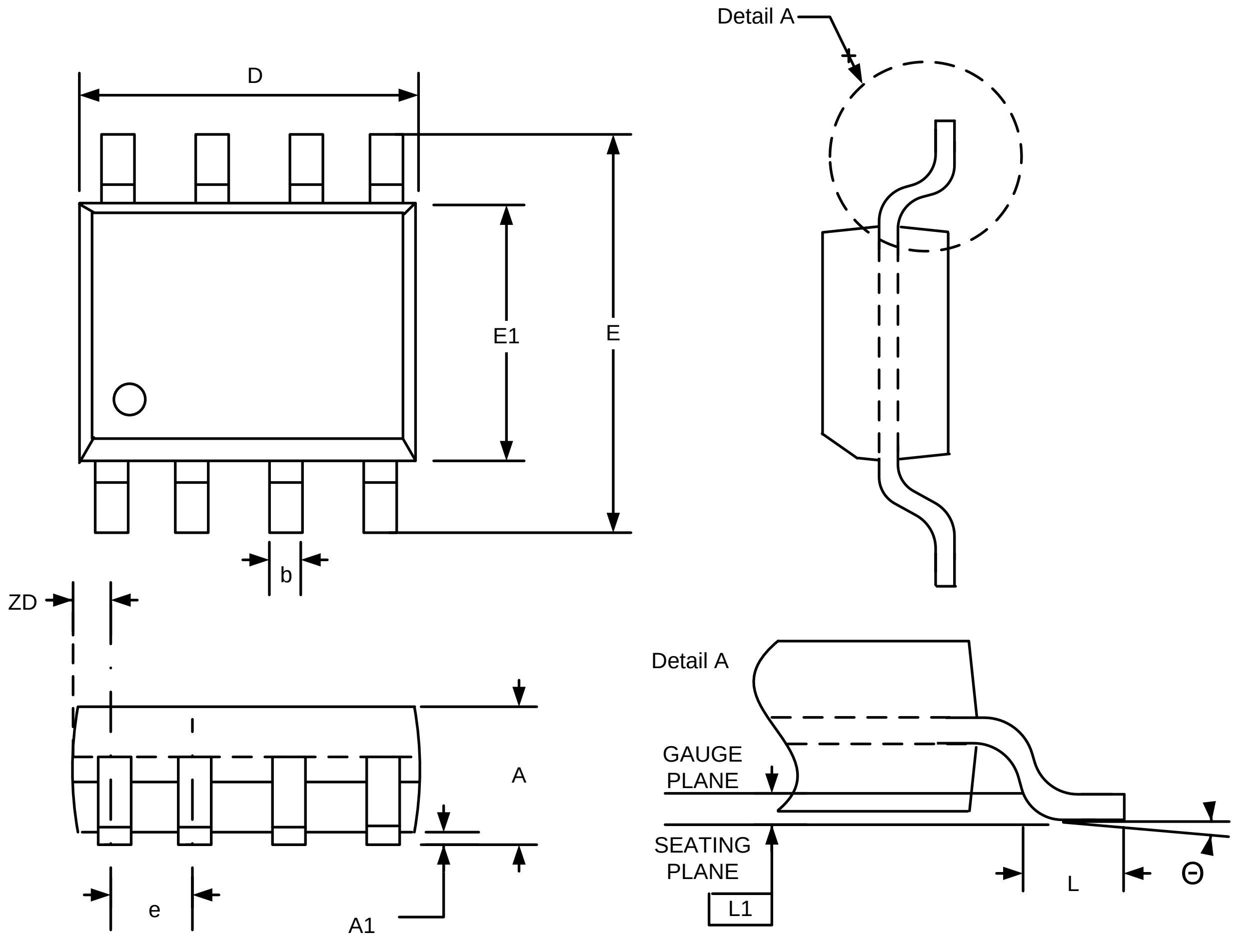
8.4 UDFN Package

GT: Giantec Logo
33: Part Number GT93C76-2UDLI-TR
YWW: Date Code, Y=year, WW=week

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline

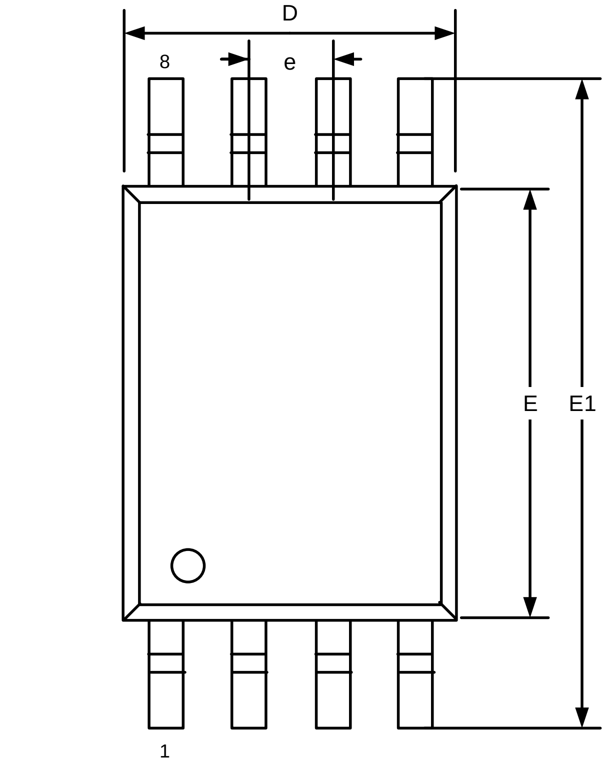


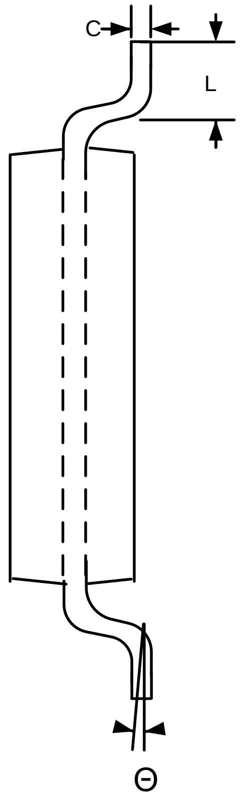
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

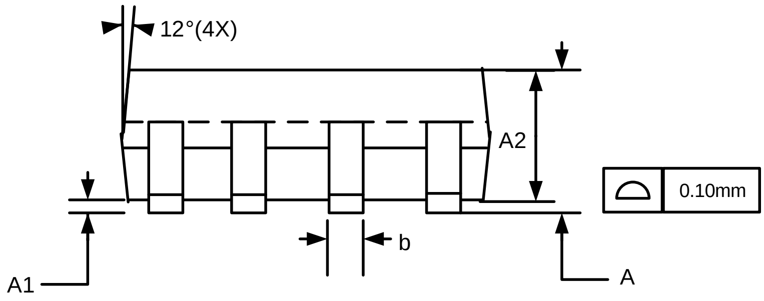
Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline





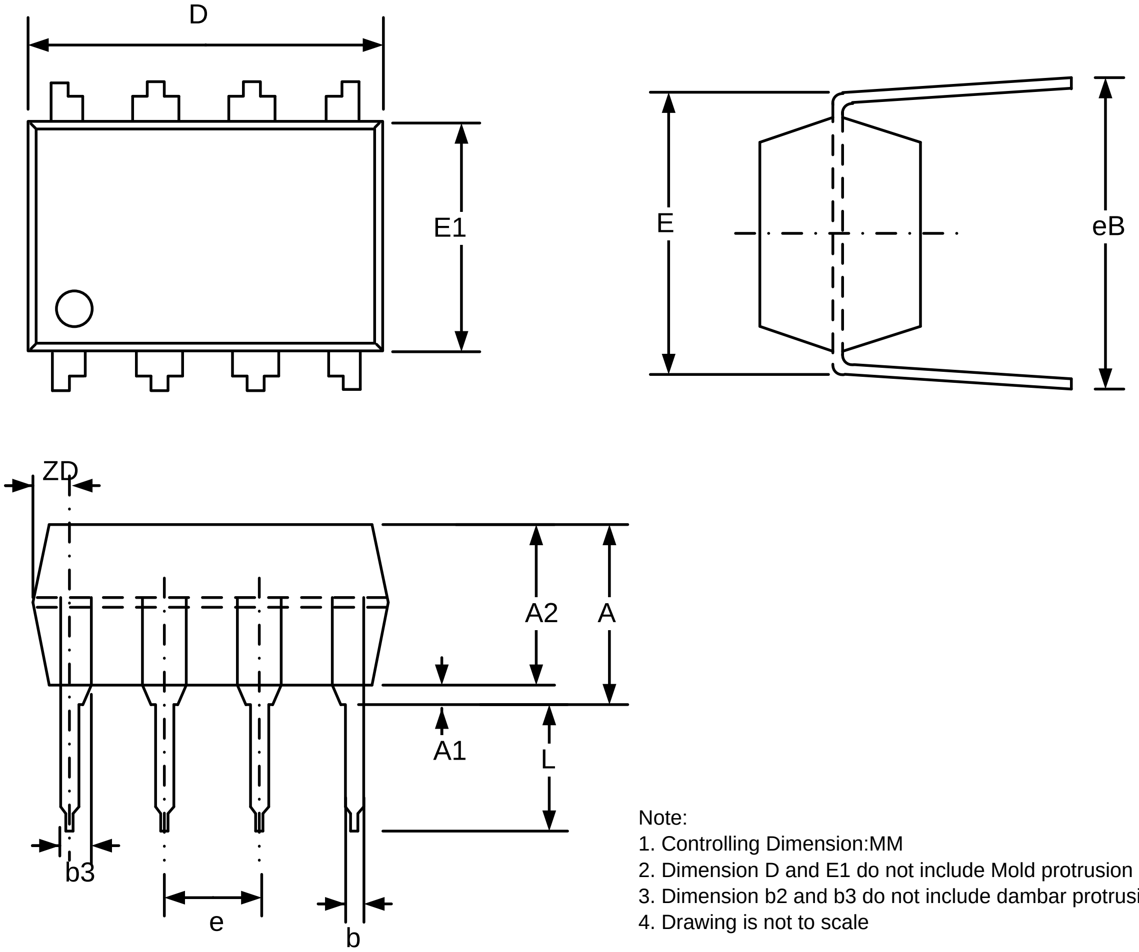


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

9.3 PDIP

8L 300mil PDIP Package Outline

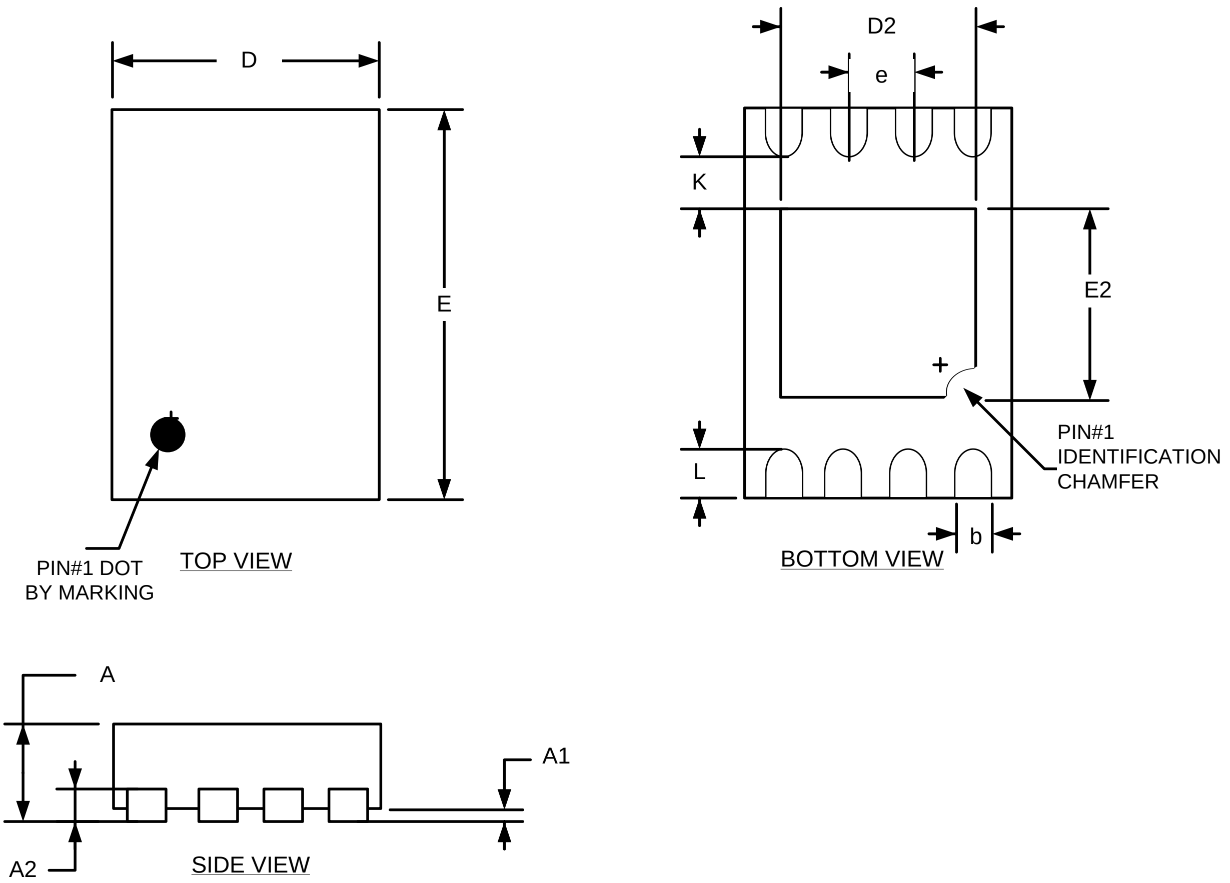


Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b2 and b3 do not include dambar protrusion/instrusion
4. Drawing is not to scale

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.60	--	4.20	0.142	--	0.165
A1	0.38	--	0.75	0.015	--	0.030
A2	3.25	--	3.45	0.128	--	0.136
b	0.36	--	0.56	0.014	--	0.022
b2	1.40	--	1.65	0.055	--	0.065
b3	0.81	--	1.17	0.032	--	0.046
D	9.01	--	9.53	0.355	--	0.375
E	7.49	--	8.26	0.295	--	0.325
E1	6.20	--	6.60	0.244	--	0.260
e	2.54 BSC.			0.100 BSC.		
eB	8.12	--	9.65	0.320	--	0.380
L	3.18	--	3.80	0.125	--	0.150
ZD	0.825 REF.			0.032 REF.		

9.4 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

10. Revision History

Revision	Date	Descriptions
A0	Nov. 2010	Initial version
C1	Oct. 2013	Revise SOIC/SOP to SOIC
C2	Jul. 2019	Update TSSOP POD and VP
C3	Sep. 2022	Update Logo and other
C4	Mar.2025	Add UDFN Package