GT25C256A

Automotive(A2)

256-Kbit

SPI Bus

EEPROM

Table of Contents

GT25C256A

1. Features

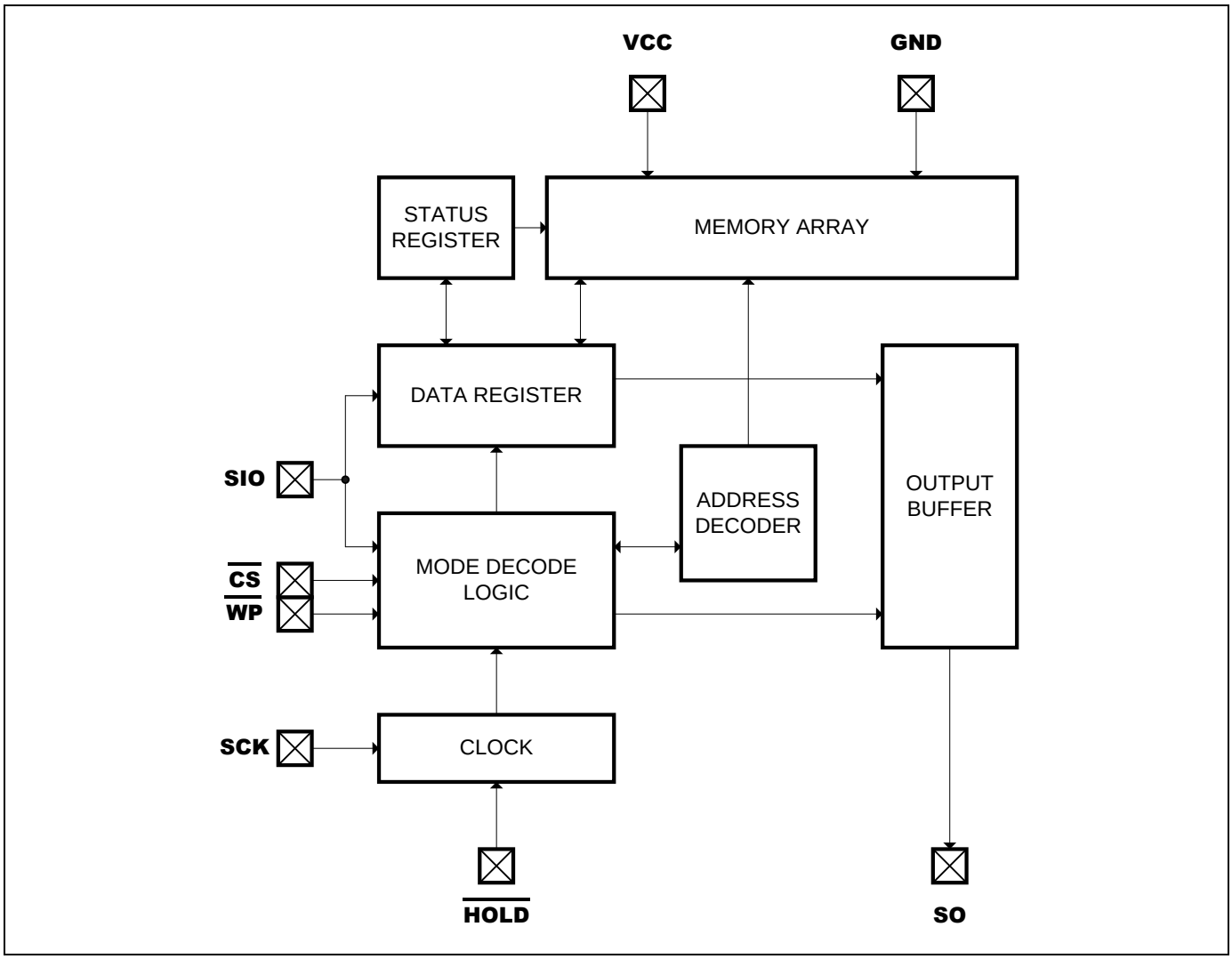
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI Modes 0
- Wide-voltage Operation:
  - VCC = 1.7V to 5.5V(-40°C to 105°C)
- Operating frequency: 20 MHz (5.5V)
- Low power CMOS
  - Standby current: ≤5 μA (5.5V)
  - Operating current: ≤5 mA (5.5V)
- Memory Organization: 256Kb (32,768 x 8)
  - Byte and Page write (up to 128 bytes)
  - Partial page write allowed
- Block Write Protection
  - Protect Entire Array
- Self timed write cycle: 5 ms (max.)
- High Product Endurance
  - Endurance: 4 million cycles at 25°C
  - Data retention: 100 years at 25°C
- Compliant with automotive standard AEC-Q100 grade 2
- Packages (8-pin): SOIC, TSSOP and UDFN
- Lead-free, RoHS, Halogen free, Green
- With ECC function

2. General Description

The GT25C256A is an automotive standard electrically erasable programmable read only memory (EEPROM) product. The GT25C256A contains a memory array of 256Kb (32,768 x 8), which is organized in 128 bytes per page.

This EEPROM operates in a wide voltage range from 1.7V to 5.5V, which fits most application. The product is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOP, TSSOP and UDFN. The GT25C256A has a compatible SPI interface: Chip-Select ($\overline{CS}$), Serial Data In (SI), Serial Data Out (SO) and Serial Clock (SCK) for high-speed communication. Furthermore, a Hold feature via $\overline{HOLD}$ pin allows the device entering into a suspended state whenever necessary and resuming the communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism and device status monitoring. In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is implemented. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into Standby mode. This should also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

3. Functional Block Diagram



Serial Interface Description

Master: The device that provides a clock signal.

Slave: GT25C256A.

Transmitter/Receiver: The GT25C256A has data input (SI) and data output (SO).

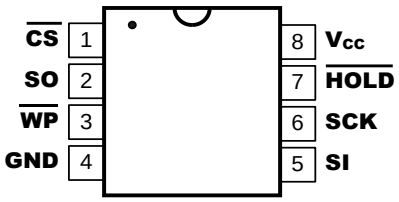
MSB MSB (Most Significant Bit) is the first bit being transmitted or received.

Op-Code: Operational instruction code typically sent to the GT25C256A is the first byte of information transmitted after $\overline{CS}$ is Low. If the Op-Code is a valid instruction as listed in Table 5.4, then it will be decoded appropriately. It is prohibited to send an invalid Op-Code.

4. Pin Configuration

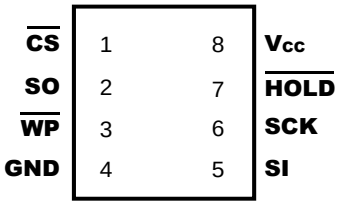
4.1 8-Pin SOIC and TSSOP

Top View



4.2 8-Lead UDFN

Top View



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	$\overline{CS}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{WP}$	I	Write Protect Input
4	GND	-	Ground
5	SI	I	Serial Data Input
6	SCK	I	Serial Clock
7	$\overline{HOLD}$	I	Hold function
8	V_{CC}	-	Supply Voltage

4.4 Pin Descriptions

Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is used to enable or disable the device. Upon power-up, $\overline{CS}$ must follow the supply voltage. When the device is ready for instruction input, this signal requires a High-to-Low transition. Once $\overline{CS}$ is stable at Low, the device is enabled. Then the master and slave can communicate among each other through SCK, SI, and SO pins. Upon completion of transmission, $\overline{CS}$ must be driven to High in order to stop the operation or start the internal write operation. And the device will enter into standby mode, unless an internal write operation is in progress. During this mode, SO becomes high impedance.

Serial Clock (SCK) [1]

Under the SPI modes (0, 0), this clock signal provides synchronization between the master and GT25C256A. Typically, Op-Codes, addresses and data are latched from SI at the rising edge of SCK, while data from SO/SI are clocked out at the falling edge of SCK.

Note: [1] Mode 3 is not supported

Serial Data Input (SI)

Data Input pin.

Serial Data Output (SO)

Data output pin.

Write Protect ($\overline{WP}$)

This active Low input signal is utilized to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being modified. To activate the Hardware Write Protection, $\overline{WP}$ must be Low simultaneously when WPEN is set to 1.

Hold ($\overline{HOLD}$)

This feature is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). The $\overline{HOLD}$ signal transitions must occur only when SCK is Low and be held stable during SCK transitions. Connecting $\overline{HOLD}$ to High disables this feature. Figure. 5-8 shows Hold timing.

Note: $\overline{HOLD}$ cannot be powered on earlier than Vcc, and

the amplitude of $\overline{\text{HOLD}}$ cannot be greater than Vcc.

5. Device Operation

5.1 Status Register

The Status Register accessible by the user consists of 8-bits data for write protection control and write status. It becomes Read-Only under any of the following conditions: Hardware Write Protection is enabled or WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Table 5.1: Status Register

Bit	Symbol	Name	Description
0	$\overline{\text{RDY}}$	Ready	When $\overline{\text{RDY}}$ = 0, device is ready for an instruction. When $\overline{\text{RDY}}$ = 1, device is busy. As busy, device only accepts Read Status Register command.
1	WEN	Write Enable	This represents the write protection status of the device. When WEN = 0, Status Register and entire array cannot be modified, regardless the setting of WPEN, $\overline{\text{WP}}$ pin or block protection. Write Enable command (WREN) can be used to set WEN to 1. Upon power-up stage, WEN is reset to 0.
2	BP0	Block Protect Bit	Despite of the status on WPEN, $\overline{\text{WP}}$ or WEN, BP0, BP1 and BP2 configure any combinations of the corresponding blocks being protected (Table 5.2). They are non-volatile memory and programmed to 0 by factory.
3	BP1	Block Protect Bit	
4	BP2	Block Protect Bit	
5	X	Don't Care	Values can be either 0 or 1, but are not retained. Mostly always 0, except during write operation.
6	X	Don't Care	
7	WPEN	Write Protect Enable	This bit can be utilized to enable Hardware Write Protection, together with $\overline{\text{WP}}$ pin. If enabled, Status Register becomes read-only. However, the memory array is not protected by this mode. Hardware Write Protection requires the setting of $\overline{\text{WP}}$ = 0 and WPEN = 1. Otherwise, it is disabled. WPEN cannot be altered from 1 to 0 if $\overline{\text{WP}}$ is already set to Low. (Table 5.3 for write protection).

Note:

1, During internal write cycles, bits 0 to bit 7 are temporarily 1's.

2, After performing the write operation, the Ready bit may appear at any position from bit 0 to bit 7 when it first changes from 1b to 0b. When reading this result, Master needs to read the register again to read the correct value.

3, The method of delaying reading the register by 5ms after the write operation is also recommended.

Table 5.2: Block Protection by BP0, BP1 and BP2

Level	Status Register Bits			Array Addresses Protected
	BP2	BP1	BP0	
0	Not used	0	0	None
1	Not used	0	1	None
2	Not used	1	0	None
3 (All)	Not used	1	1	0000h-7FFFh

Table 5.3: Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

5.2 Op-Code Instructions

The operations of the GT25C256A are controlled by a set of instruction Op-Codes (Table 5.4 that are clocked-in serially via SI pin. To initiate an instruction, the chip select ($\overline{CS}$) must be Low. Subsequently, each Low-to-High transition of the clock (SCK) will latch a stable level from SI. After the 8-bit Op-Code, it may continue to latch-in an address and/or data from SI accordingly, or to output data from SO. During data output, data are latched out at the falling edge of SCK. All communications start with MSB first. Upon the transmission of the last bit but prior to any following Low-to-High transition on SCK, $\overline{CS}$ must be brought to High in order to end the transaction and start the operation. The device will enter into Standby Mode after the operation is completed.

Table 5.4: Instruction Op-Codes[1,2]

Name	Op-Code	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch/Exit OTP Mode
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Array at Normal Read Mode
WRITE	0000 X010	Write Data to Memory Array

Notes: [1] X = Don't care bit. However, it is recommended to be "0".

[2] It is strongly recommended that an appropriate format of Op-Code must be entered. Otherwise, it may cause unexpected phenomenon to be occurred. Nevertheless, it is illegal to input invalid any Op-Code.

Table 5.5: Address Key

Name	GT25C256A
A_N	A_{15}-A_0

5.3 Write Enable

When V_{CC} is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR) or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a Write Enable (WREN) instruction is necessary to set WEN to 1 (Figure. 5-2).

5.4 Write Disable

The device can be completely protected from modification by resetting WEN to 0 through the Write Disable (WRDI) instruction (Figure. 5-3).

5.5 Read Status Register

The Read Status (RDSR) instruction reviews the status of Write Protect Enable, Block Protection setting, Write Enable state and $\overline{RDY}$ status (Table 5.1). These 8 bits information can be repeatedly output on SO after the initial Op-Code (Figure. 5-4). It is recommended that the status of Write Enable and $\overline{RDY}$ be checked, especially prior to an attempted modification of data.

RDSR is the only instruction accepted when an internal write cycle is underway. Bits 0~7 are ones during an internal write cycle.

5.6 Write Status Register

The Write Status Register (WRSR) instruction allows the user to choose a Block Protection setting and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1 and are not stored in the Status Register. WRSR will be ignored unless both following conditions are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled (Refer to Table 5.3). Except for $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is completed and the register is updated. Note that WPEN can be changed from 1 to 0 only if $\overline{WP}$ is already set High. Once completed, WEN is reset for complete chip write protection (Fig. 5-5).

5.7 Read Data

This instruction includes an Op-Code and 16-bit address, then results the selected data to be shifted out from SO. Following the first data byte, additional sequential data can be output. If the data byte of the last address is initially output, then address will rollover to the first address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal ceases the operation (Figure. 5-6).

5.8 Write Data

The WRITE instruction contains an Op-Code, a 16-bit address and the first data byte. Additional data bytes may be supplied sequentially after the first byte. Each WRITE instruction can affect up to 128 bytes of data in a page. Each page has a starting address XXXXXXXX X0000000 and an ending address XXXXXXXX X1111111. After the last byte of data in a page is input, the address rolls over to the beginning of the same page. If more than 128 bytes of data is input during a single instruction, then only the last 128 bytes will be retained, but the initial data will be overwritten.

The contents of the array defined by Block Protection cannot be modified as long as that block configuration is selected. The contents of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction is initiated prior to WRITE. Once Write operation is completed, WEN is reset for complete chip write protection (Figure. 5-7). Besides, Hardware Write Protection has no affect on the memory array.

5.9 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes [1]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written independently. In this case, the ECC function also writes the three other bytes located in the same group [1]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in 6.4 Reliability.

Note: 1. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

5.10. Diagrams

Figure 5-1. Synchronous Data Timing

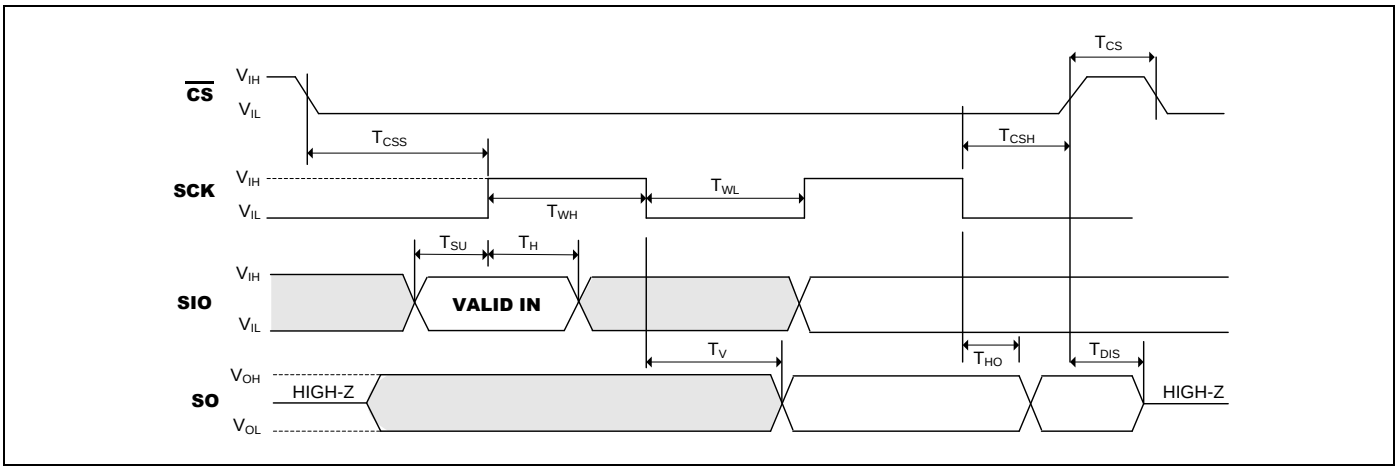


Figure 5-2. WREN Timing

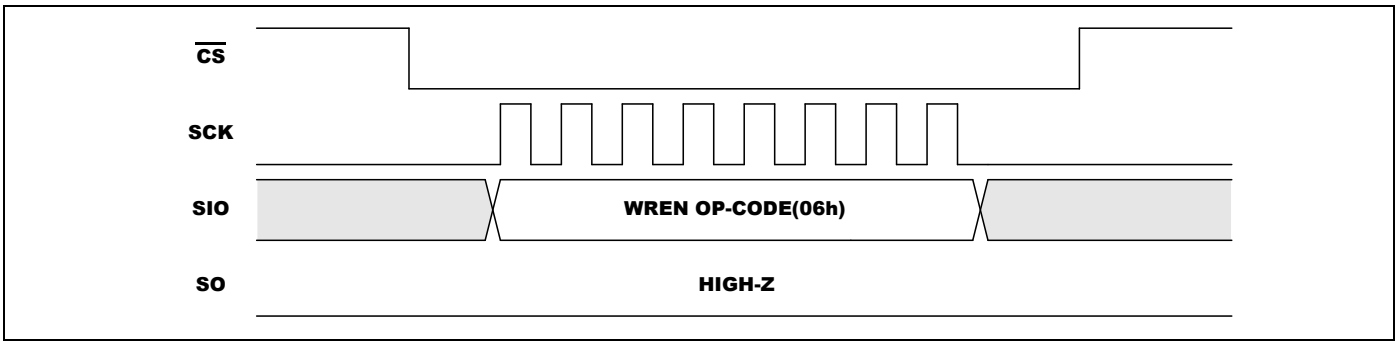


Figure 5-3. WRDI Timing

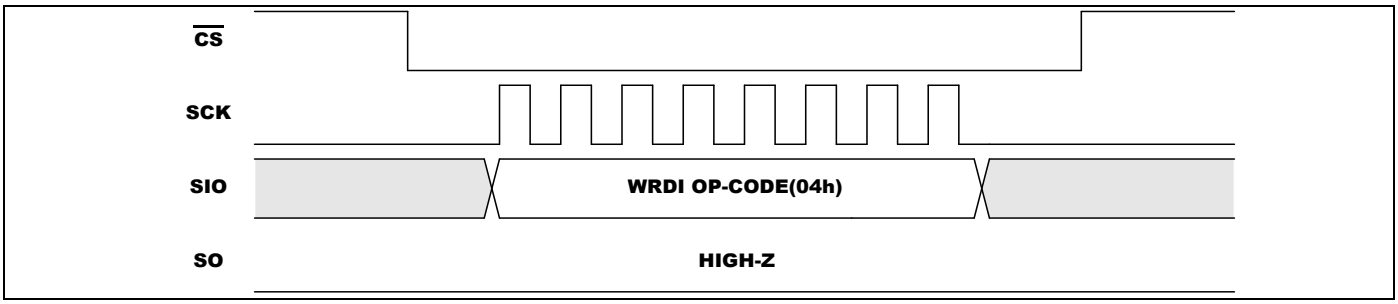


Figure 5-4. RDSR Timing

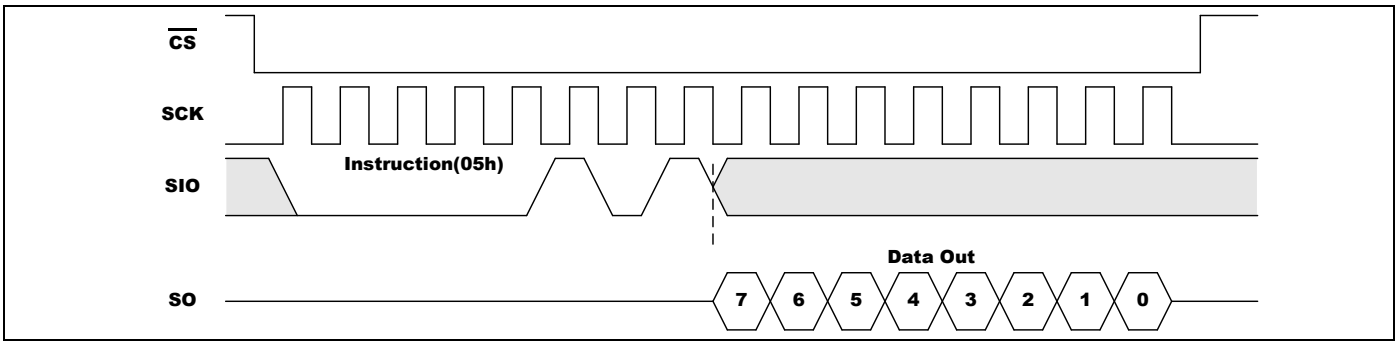


Figure 5-5. WRSR Timing

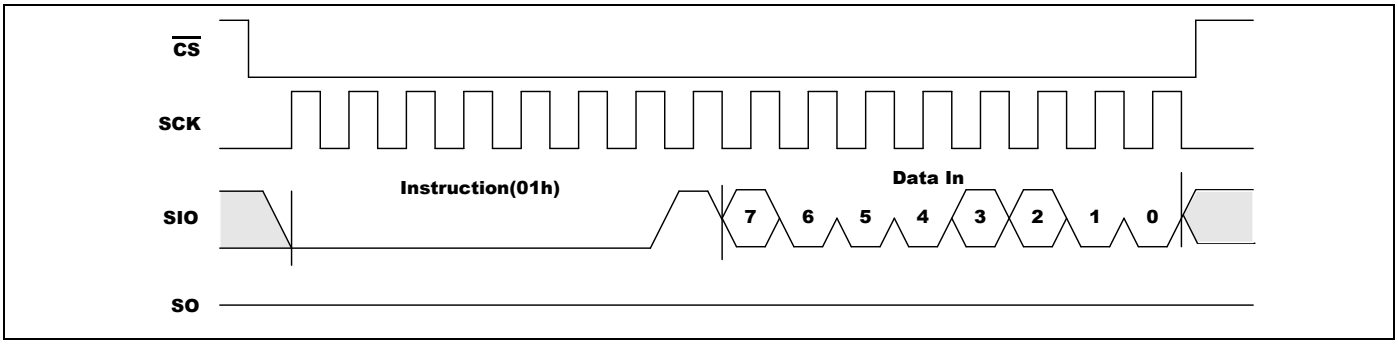
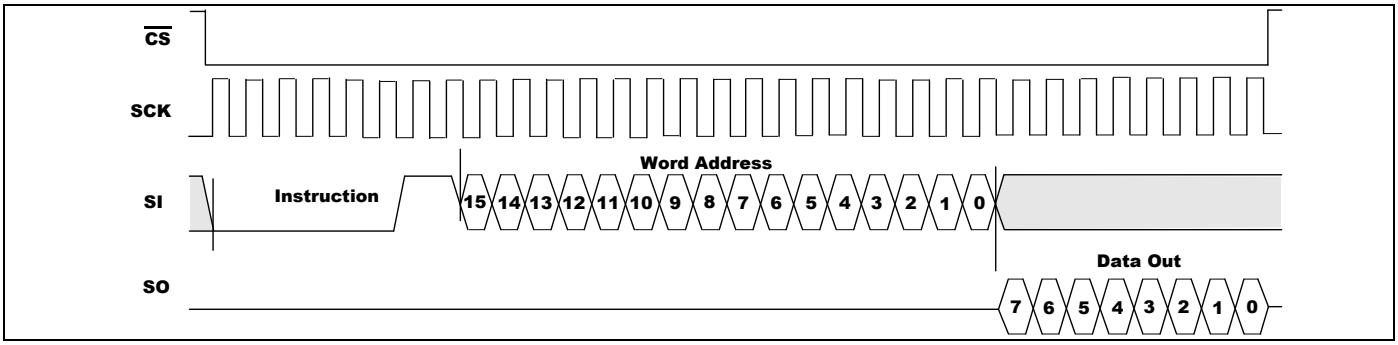
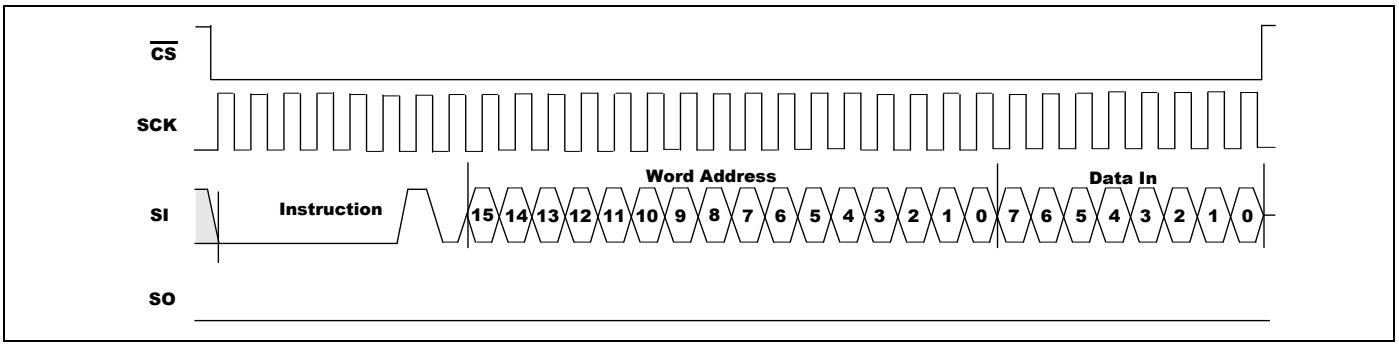


Figure 5-6. Read Timing



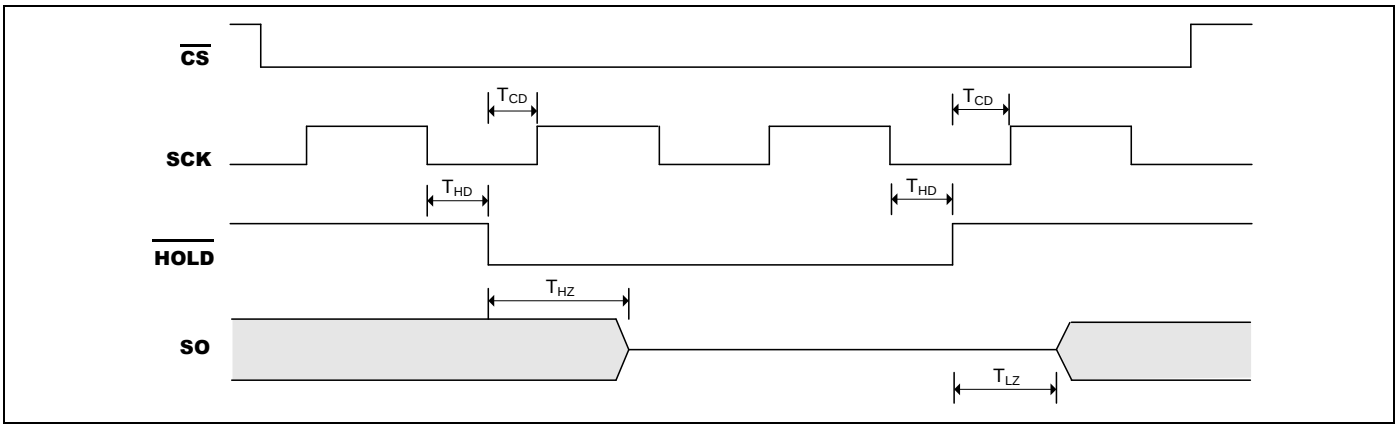
Address Bit15 must set 0

Figure 5-7. Write Timing



Address Bit15 must set 0

Figure 5-8. HOLD Timing



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive Grade 2	–40°C to +105°C	1.7V to 5.5V

6.3 Reliability

Ambient Temperature (TA)	Symbol	Parameter	Min.	Unit
Ta=+25°C	End	Endurance	4 million	Program / Erase Cycles
	DR	Data Retention	100	Years

Note: [1] The write cycle endurance is defined for group of four bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer. The Write cycle endurance is defined by characterization and qualification.

[2]A Write cycle is executed when either a Page Write or a Byte write is decoded. When using the Byte Write or the Page Write, refer also to 5.9 ECC (Error Correction Code) and Write cycling

6.4 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	-	6	pF
$C_{I/O}$	Input / Output Capacitance	-	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

6.5 DC Electrical Characteristic

Automotive: T_A = –40°C to +105°C, V_{CC} = 1.7V ~ 5.5V

Symbol	Parameter	Vcc	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage			1.7	5.5	V
V_{IH}	Input High Voltage			0.7* V_{CC}	V_{CC}+0.5	V
V_{IL}	Input Low Voltage			-0.3	0.3* V_{CC}	V
I_{LI}	Input Leakage Current		V_{IN} = 0V To V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current		V_{OUT} = 0V To V_{CC}, $\overline{CS}$ = V_{CC}	-2	2	µA
V_{OH1}	Output High Voltage	1.7	I_{OH} = -0.4mA	0.8*V_{CC}	—	V
		5.5	I_{OH} = -2 mA	0.8*V_{CC}	—	V
V_{OL1}	Output Low Voltage	1.7	I_{OL} = 1.5 mA	—	0.4	V
		5.5	I_{OL} = 2 mA	—	0.4	V
I_{CC1}	Write Operating Current	1.7	Write at 3 MHz, SO=Open	—	1.5	mA
		5.5	Write at 20 MHz, SO=Open	—	2.0	mA
I_{CC2}	Read Operating Current	1.7	Read at 3 MHz, SO=Open	—	3	mA
		5.5	Read at 20 MHz, SO=Open	—	5	mA
I_{SB}	Standby Current	1.7	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	3	µA
		5.5	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	5	µA

6.6 AC Electrical Characteristic

Automotive: T_A = –40°C to +105°C, Supply voltage = 1.7V to 5.5V

Symbol	Parameter[1]	1.7V≤Vcc<2.5V		2.5V≤Vcc<4.5V		4.5V≤Vcc≤5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCK}	SCK Clock Frequency	0	3	0	10	0	20	MHz
T_{RI}	Input Rise Time	—	1	—	1	—	1	μs
T_{FI}	Input Fall Time	—	1	—	1	—	1	μs
T_{WH}	SCK High Time	80	—	40	—	20	—	ns
T_{WL}	SCK Low Time	80	—	40	—	20	—	ns
T_{CS}	$\overline{CS}$ High Time	100	—	50	—	25	—	ns
T_{CSS}	$\overline{CS}$ Setup Time	100	—	50	—	25	—	ns
T_{CSH}	$\overline{CS}$ Hold Time	100	—	50	—	25	—	ns
T_{SU}	Data In Setup Time	20	—	10	—	5	—	ns
T_H	Data In Hold Time	20	—	10	—	5	—	ns
T_{HD}	$\overline{HOLD}$ Setup Time	20	—	10	—	5	—	ns
T_{CD}	$\overline{HOLD}$ Hold Time	20	—	10	—	5	—	ns
T_V[2]	Output Valid	0	80	0	40	0	20	ns
T_{HO}	Output Hold Time	0	—	0	—	0	—	ns
T_{LZ}	$\overline{HOLD}$ to Output Low Z	0	80	0	40	0	25	ns
T_{HZ}	$\overline{HOLD}$ to Output High Z	—	80	—	40	—	40	ns
T_{DIS}	Output Disable Time	—	80	—	40	—	40	ns
T_{WC}	Write Cycle Time	—	5	—	5	—	5	ms

Notes: [1] The parameters are characterized but not 100% tested.

[2]C_L = 30pF (typical)

7. Ordering Information

Automotive Grade: -40°C to +105°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.7V to 5.5V	GT25C256A-2GLA2-TR	150-mil SOIC
	GT25C256A-2ZLA2-TR	3 x 4.4 mm TSSOP
	GT25C256A-2UDLA2-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel “-TR” (4K per reel), except UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.

8. Top Markings

8.1 SOIC Package

G: Giantec Logo

5256A2GX: GT25C256A-2GLA2-TR

YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package

GT: Giantec Logo

5256A2ZX: GT25C256A-2ZLA2-TR

YWW: Date Code, Y=year, WW=week

8.3 UDFN Package

GT: Giantec Logo

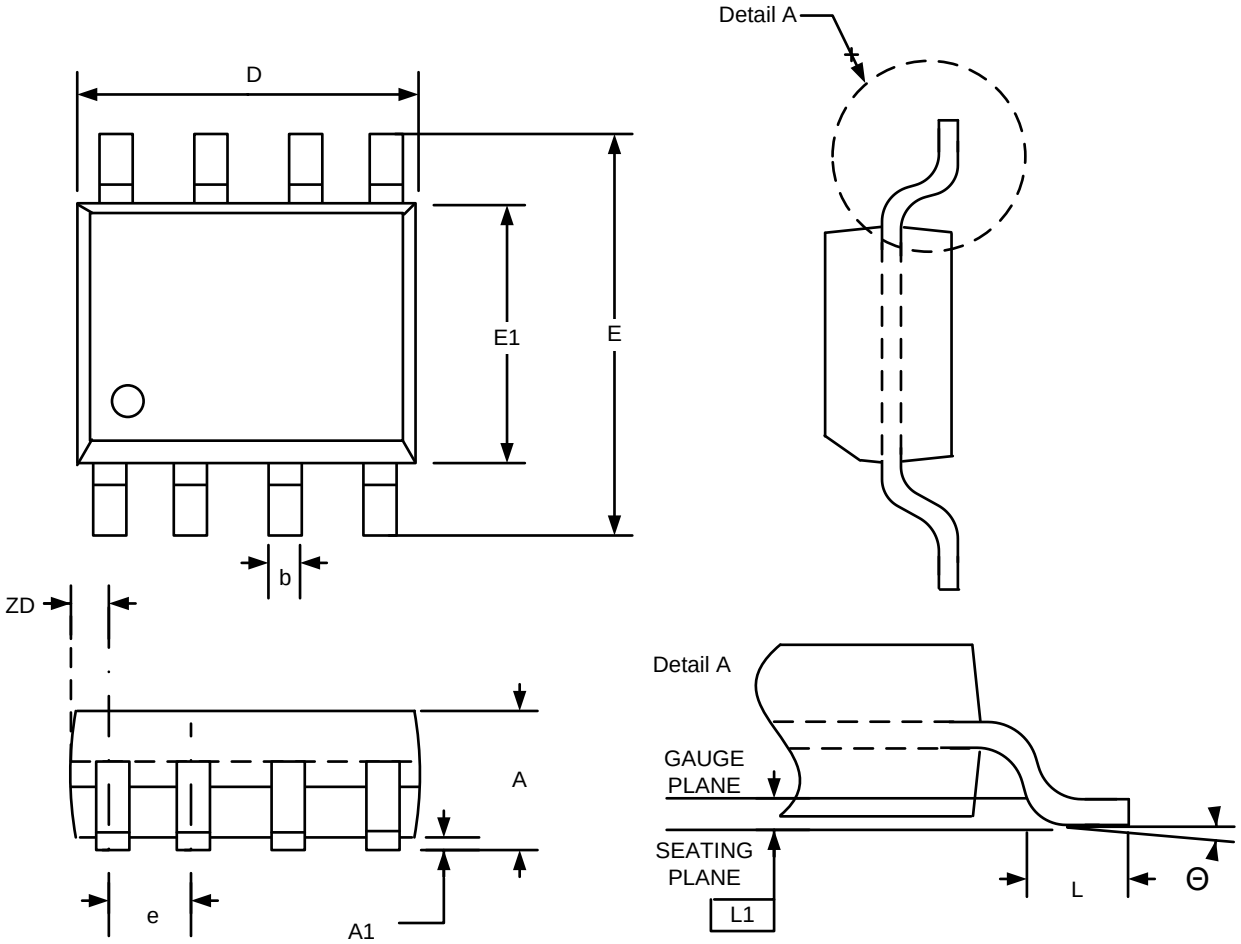
58A2: GT25C256A-2UDLA2-TR

YWW: Date Code, Y=year, WW=week

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline



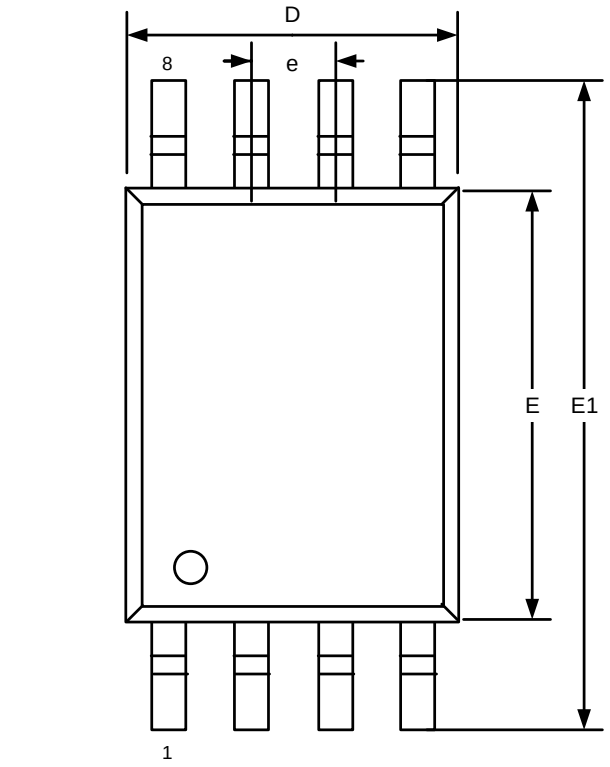
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

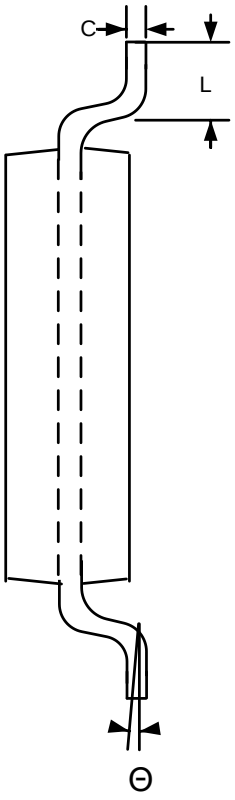
Note:

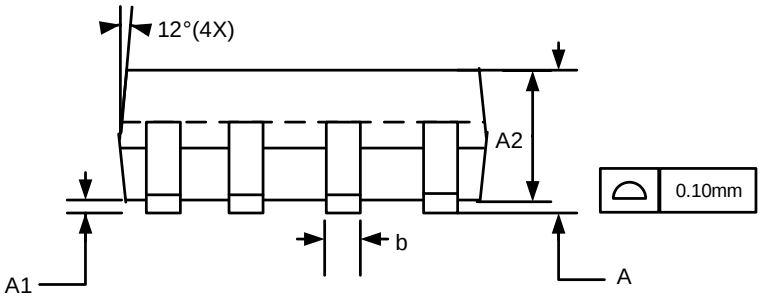
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline





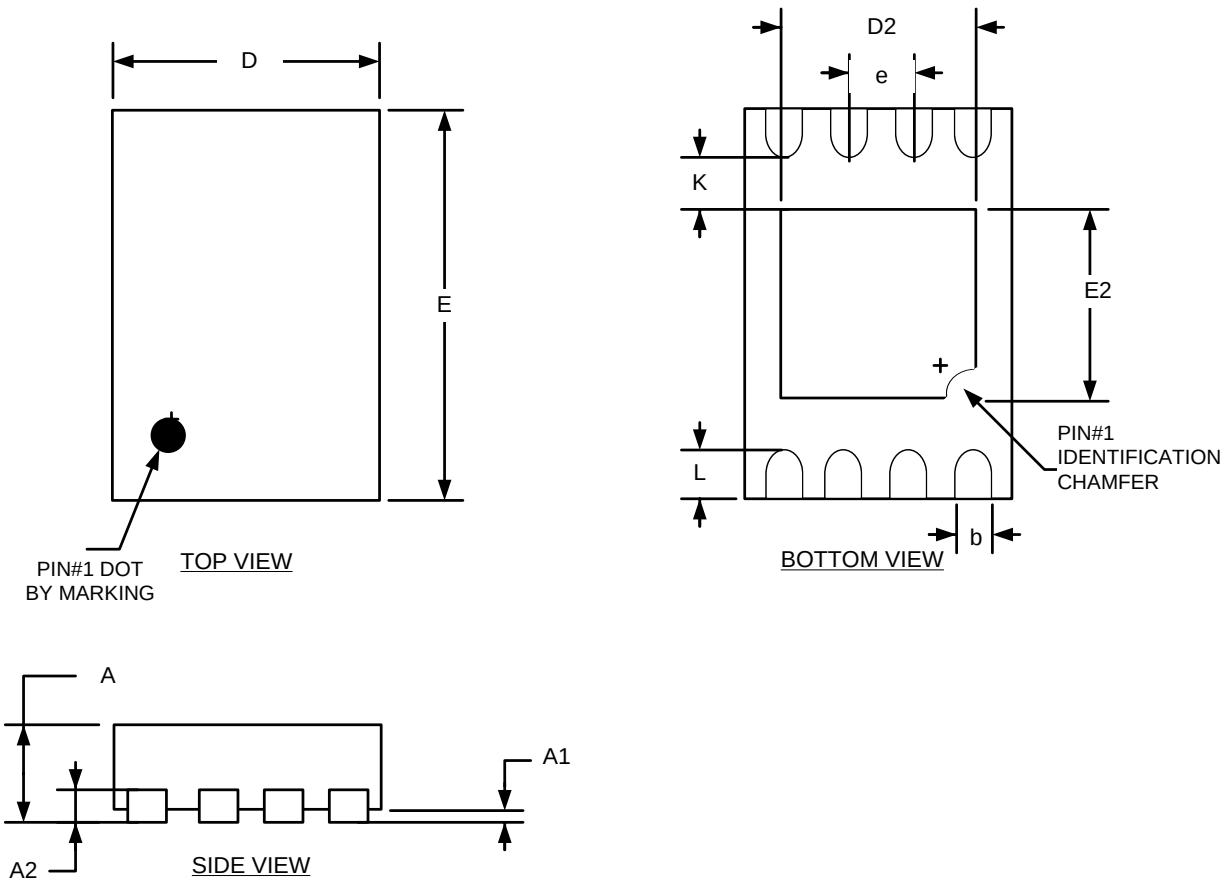


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

9.3 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

10. Revision History

Revision	Date	Descriptions
V0	Mar. 2017	Initial version
V1	May. 2022	Update Logo and other
V2	Feb. 2023	Update I_{SB}
V3	Mar. 2023	Add note for $\overline{\textbf{HOLD}}$ in 4.4
V4	June.2024	Update SPI does not support mode 3 and other issues
V5	Aug.2024	Add some notes in Table 5.1
V6	Aug.2024	Update SCK Clock Frequency(1.7V≤VCC<2.5V) changed from 4MHZ to 3MHZ