GT93C66A

Automotive (A2)

Microwire

4K Bits EEPROM

GT93C66A

Table of Contents

GT93C66A

1. Features

- Industry-standard Microwire Interface
- Wide-voltage Operation
    - V_{CC} = 2.5V to 5.5V
- Speed
    - 2 MHz (2.5V~5.5V), 3 MHz (4.5V~5.5V)
- Standby current
    - 15uA (max.) 5.5V
- Operating current
    - 2mA (max.) 5.5V
- User Configured Memory Organization
    - 256x16-bit (ORG = V_{CC} or Floating)
    - or 512x8-bit (ORG = 0V)
- Self timed write cycle: 5 ms (max.)
- Hardware and software write protection
    - Defaults to write-disabled state at power-up
    - Software instructions for write-enable/disable

- CMOS technology
- Versatile, easy-to-use interface
    - Automatic erase-before-write
    - Programming status indicator
    - Byte, Word and chip single erasable
    - Chip select enables power savings
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
    - Endurance: 1 million cycles
    - Data retention: 100 years
- Compliant with automotive standard AEC-Q100 grade 2
- Packages: SOIC and TSSOP
- Lead-free, RoHS, Halogen free, Green

2. General Description

The GT93C66A is 4kb non-volatile serial EEPROM with memory array of 4,096 bits. The array can be organized as either 512 bytes of 8 bits or 256 words of 16 bits via the ORG control. Utilizing the CMOS design and process, these products provide low standby current and low power operations. The devices can operate in a wide supply voltage range from 2.5V to 5.5V, with frequency up to 3MHz, which is recommended in automotive application.

When the ORG pin is connected to V_{CC} or floating, x16 is selected. Conversely, when it is connected to ground, x8 is chosen.

An instruction Op-code defines the various operations of the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all write and erase instructions are merely accepted while the device is in write enable mode. A selected x8 byte or x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the WRITE ALL or ERASE ALL instruction can program or erase the entire array, respectively. Once a device begins its self-timed program procedure, the data out pin (D_{OUT}) can indicate the READY/BUSY status by raising chip select (CS). The devices can output any number of consecutive bytes/words using a single READ instruction.

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3. Functional Block Diagram
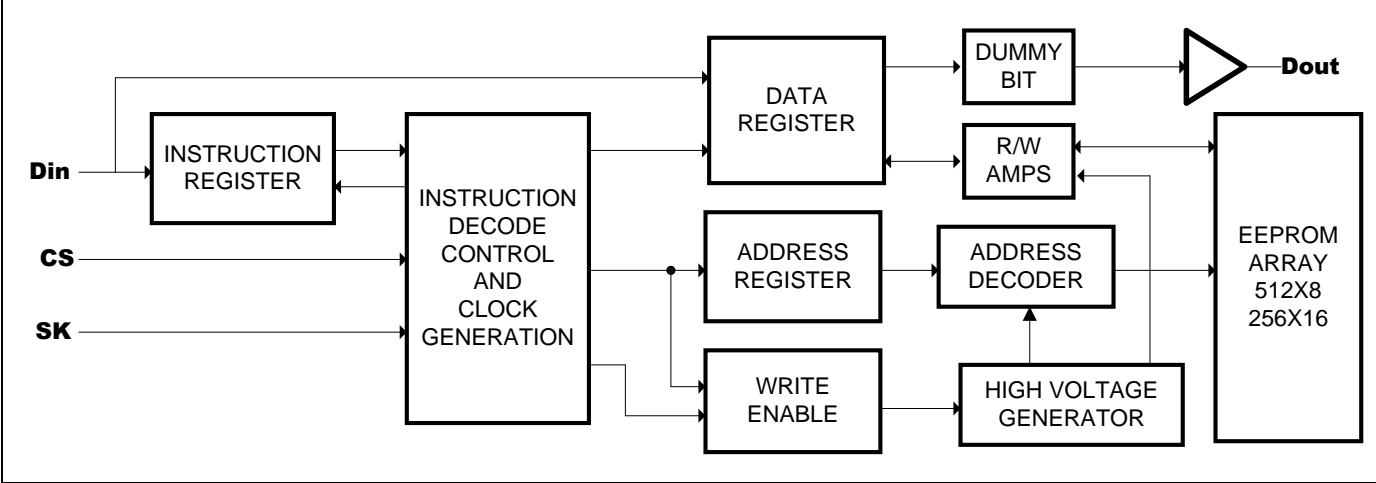
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4. Pin Configuration

4.1 8-Pin SOIC and TSSOP

Top View

```
         ┌───────┐
  CS  │1│  •    │8│  Vcc
  SK  │2│   M   │7│  NC
          A
  Din │3│  R    │6│  ORG
          K
          I
  Dout│4│  N    │5│  GND
          G
         └───────┘
```
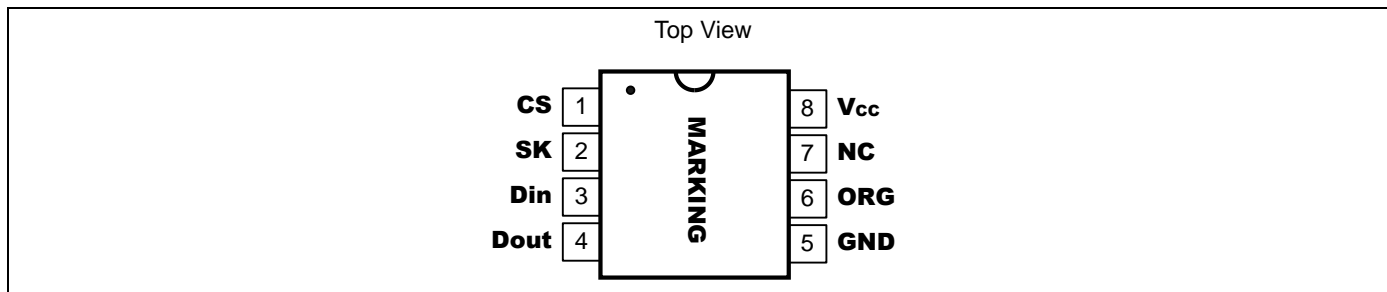
4.2 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	CS	I	Chip Select
2	SK	I	Serial Data Clock
3	D_{IN}	I	Serial Data Input
4	D_{OUT}	O	Serial Data Output
5	GND	-	Ground
6	ORG	I	Organization Select
7	NC	-	Not Connect
8	V_{CC}	-	Supply Voltage

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5. Device Operation

The GT93C66A is controlled by a set of instructions which are clocked-in serially on the D_{IN} pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the D_{IN} value must be stable at either LOW or HIGH. Each instruction begins with a start bit of the logical "1" or HIGH. Following this are the Op-code, address field, and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

5.1 Read

The READ instruction is the only instruction that outputs serial data on the D_{OUT} pin. After the read instruction and address have been decoded, data is transferred from the selected memory array into a serial shift register. (Please note that one logical "0" bit precedes the actual 8 or 16-bit output data string.) The output on D_{OUT} changes during the low-to-high transitions of SK (see Figure 5.10-2).

The GT93C66A is designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

5.2 Write Enable

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (See Figure 5.10-3) (Note: Chip select must remain LOW until

V_{CC} reaches its operational value.)

5.3 Write Disable

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

5.4 Write

The WRITE instruction writes 8 or 16 bits of data into the specified memory location. After the last data bit has been applied to D_{IN}, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN). If CS is brought HIGH, after a minimum wait of 200 ns after the falling edge of CS (T_{CS}) D_{OUT} will indicate the READY/BUSY status of the chip. Logical "0" means programming is still in progress; logical "1" means the selected memory array has been written, and the part is ready for another instruction (see Figure 5.10-4). The READY/BUSY status will not be available if the CS input goes HIGH after the end of the self-timed programming cycle (T_{wp}).

5.5 Write All Memory

The write all (WRALL) instruction programs entire memory with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (T_{CS}), the D_{OUT} pin indicates the READY/BUSY status of the chip (see Figure 5.10-5).

5.6 Erase

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of T_{CS}, will cause D_{OUT} to indicate the READ/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete

and the part is ready for another instruction (see Figure 5.10-7).

5.7 Erase All Memory

Full chip erase (ERAL) is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1" (see Figure 5.10-8).

5.8 Power-On Reset

The device incorporates a Power-On Reset (POR) circuitry which protects the internal logic against powering up into a wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This POR feature protects the device being 'brown-out' due to a sudden power loss or power cycling.

In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset (POR) circuit is embedded. During power-up, the device does not respond to any instruction until V_{CC} has reached a minimum stable level above the reset threshold voltage. Once V_{CC} passes the POR threshold, the device is reset and enters in Standby mode. This can also avoid any inadvertent Write operations during power-up stage. During power-down process, the device must enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will enter standby mode after current operation completes, provided that no internal write operation is in progress.

5.9 Instruction Set

Instruction [2]	Start Bit	OP Code	8-bit Organization (ORG = GND)			16-bit Organization (ORG = V$_{CC}$ or Floating)		
			Address[1]	Data[1]	Required Clock Cycles	Address[1]	Data[1]	Required Clock Cycles
WDS (Write Disable)	1	00	0 0xxx xxxx	—	12	00xx xxxx	—	11
WEN (Write Enable)	1	00	1 1xxx xxxx	—	12	11xx xxxx	—	11
ERAL (Erase All Memory)	1	00	1 0xxx xxxx	—	12	10xx xxxx	—	11
WRAL (Write All Memory)	1	00	0 1xxx xxxx	(D_7-D_0)	20	01xx xxxx	$(D_{15}-D_0)$	27
WRITE	1	01	(A_8-A_0)	(D_7-D_0)	20	(A_7-A_0)	$(D_{15}-D_0)$	27
READ	1	10	(A_8-A_0)	—		(A_7-A_0)	—	
ERASE	1	11	(A_8-A_0)	—	12	(A_7-A_0)	—	11

Notes: [1] x = Don't care bit.

[2] Exact number of clock cycles is required for each Op-code instruction.

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5.10 Diagrams

Figure 5.10-1. Synchronous Data Timing

Signals: CS, SK, Din, Dout (READ), Dout (WRITE) (WRALL) (ERASE) (ERAL)

Timing parameters: T_{CSS}, T_{SKH}, T, T_{SKL}, T_{CSH}, T_{DIS}, T_{DIH}, T_{PD0}, T_{PD1}, T_{DF}, T_{SV}

Status Valid

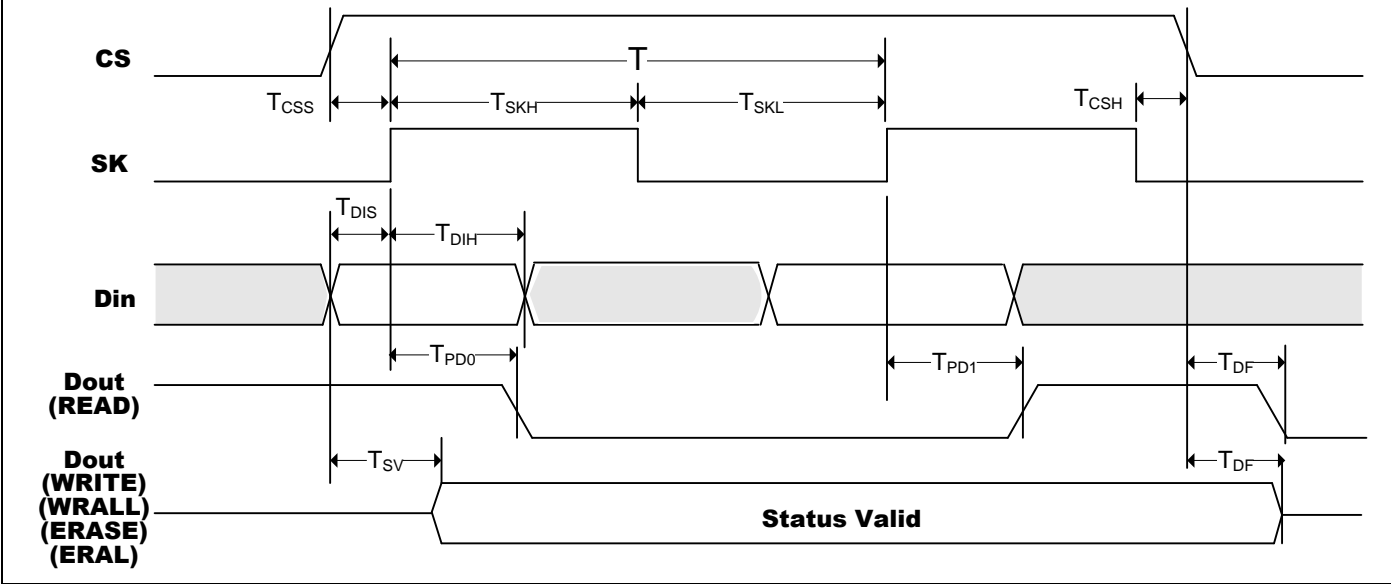### Figure 5.10-2. Read Cycle Timing

CS — T_{CS}

Din: 1 1 0 An ... A0

Dout: 0 Dm ... D0 *
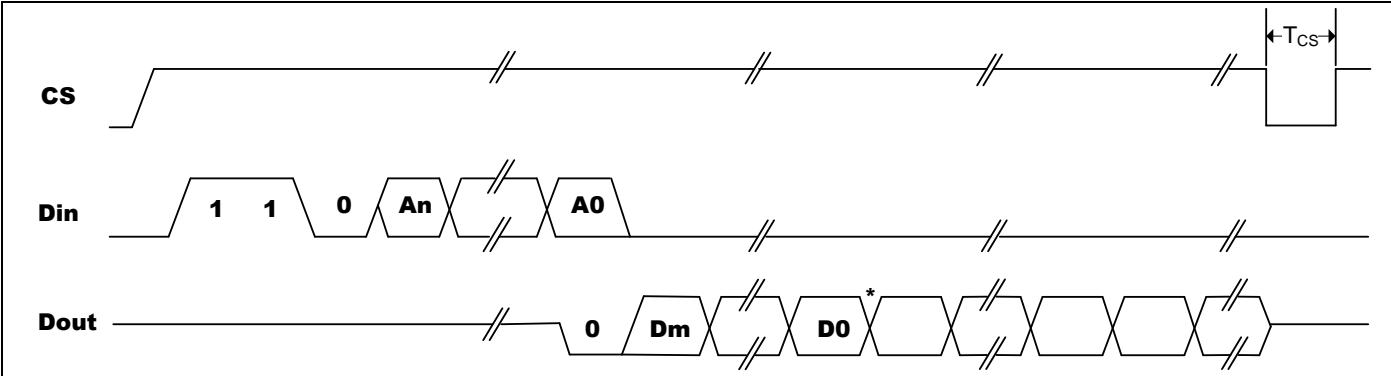
Notes: * Address Pointer Cycles to the Next Register

Figure 5.10-3. Write Enable (WEN) Cycle Timing

CS — T_{CS}

Din: 1 0 0 1 1

Dout= 3-state(Hi-Z)
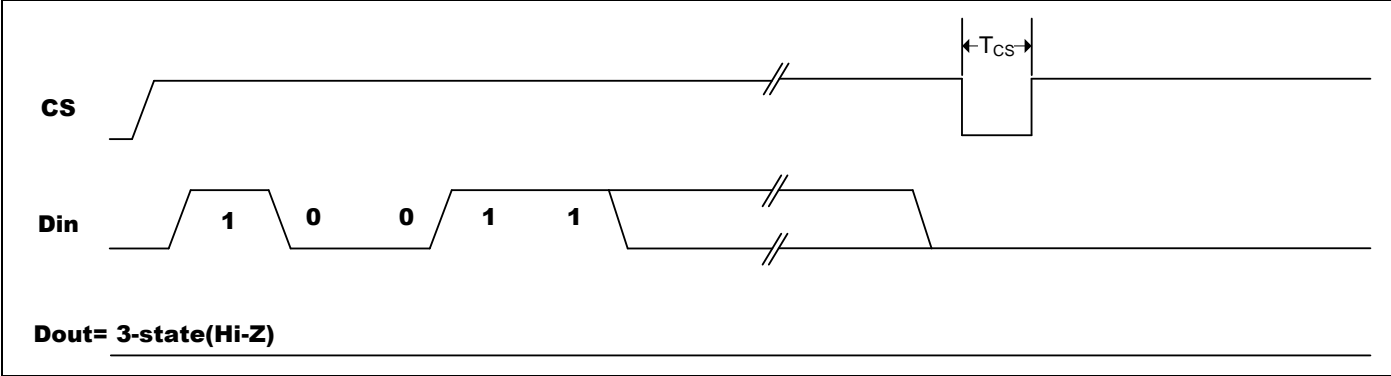
Figure 5.10-4. Write (Write) Cycle Timing

Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

[2] To determine data bits An - A0 and data bits Dm-D0, see Instruction Set for the appropriate device.

Figure 5.10-5. Write All (WRALL) Cycle Timing

Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

[2] To determine data bits Dm-D0, see Instruction Set for the appropriate device.

Figure 5.10-6. Write Disable (WDS) Timing

Giantec Semiconductor Corp   *www.giantec-semi.com*

Figure 5.10-7. Erase (Erase) Cycle Timing
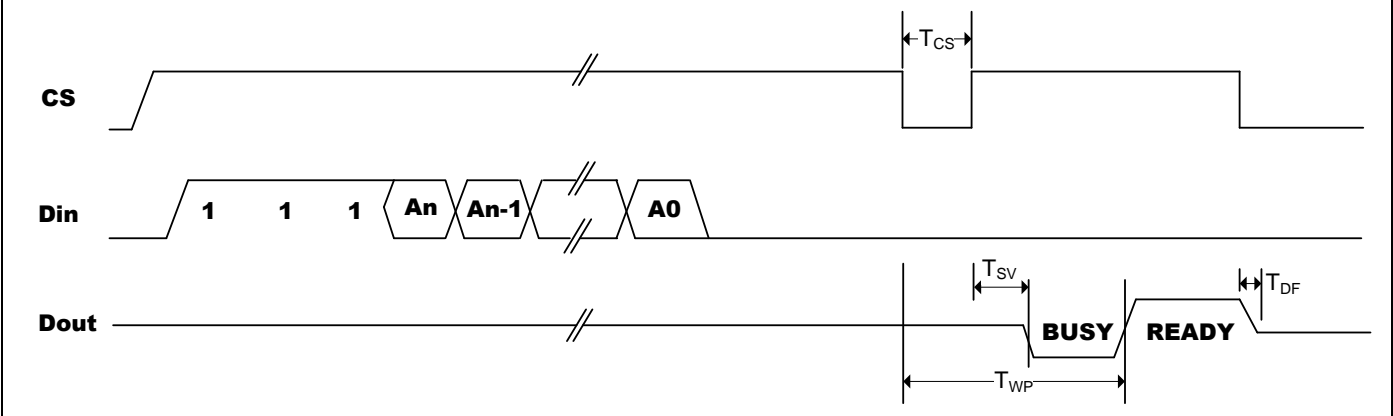
Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

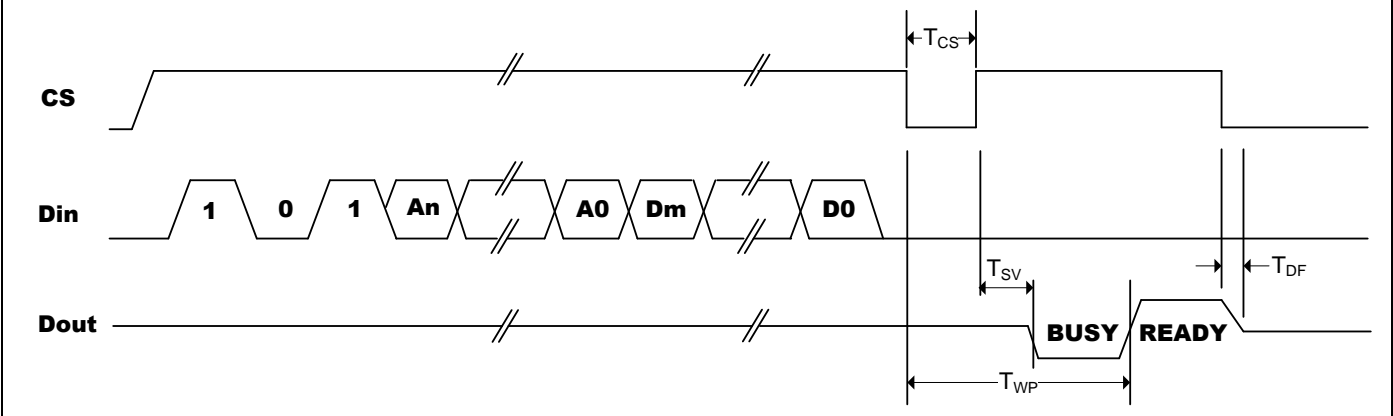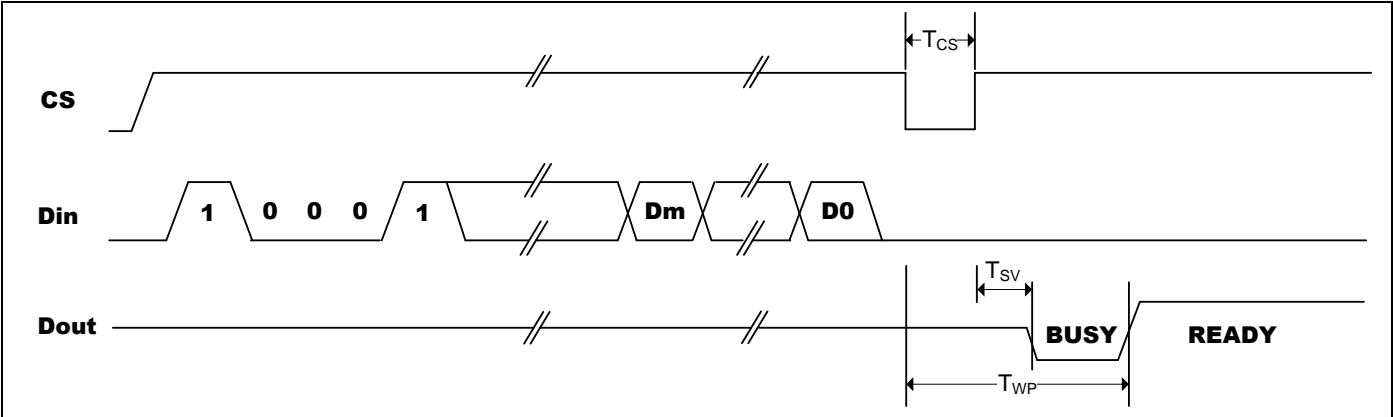[2] To determine data bits An - A0, see Instruction Set for the appropriate device.

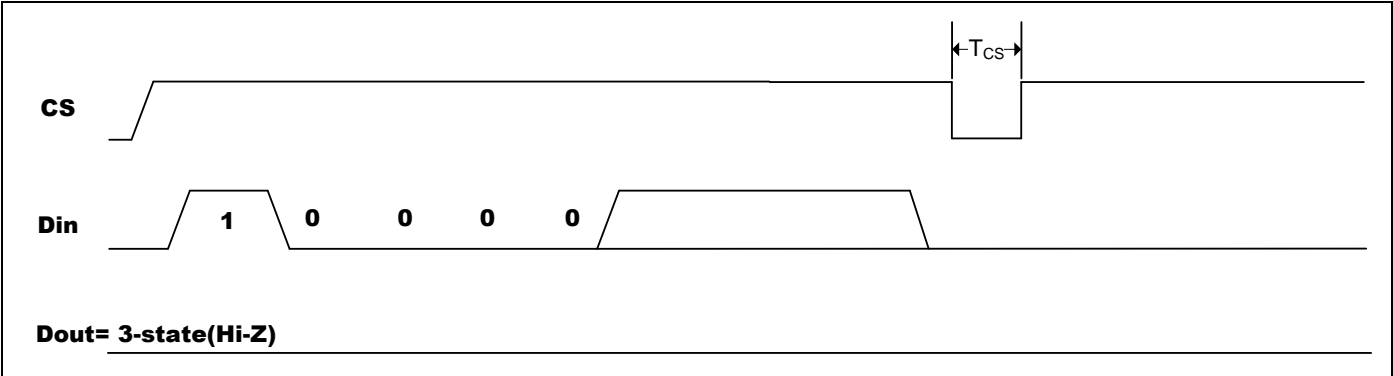### Figure 5.10-8. Erase All (ERAL) Cycle Timing

Notes: [1] After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in BUSY status (D_{OUT} indicates BUSY status) then attempting to perform another instruction could cause device malfunction.

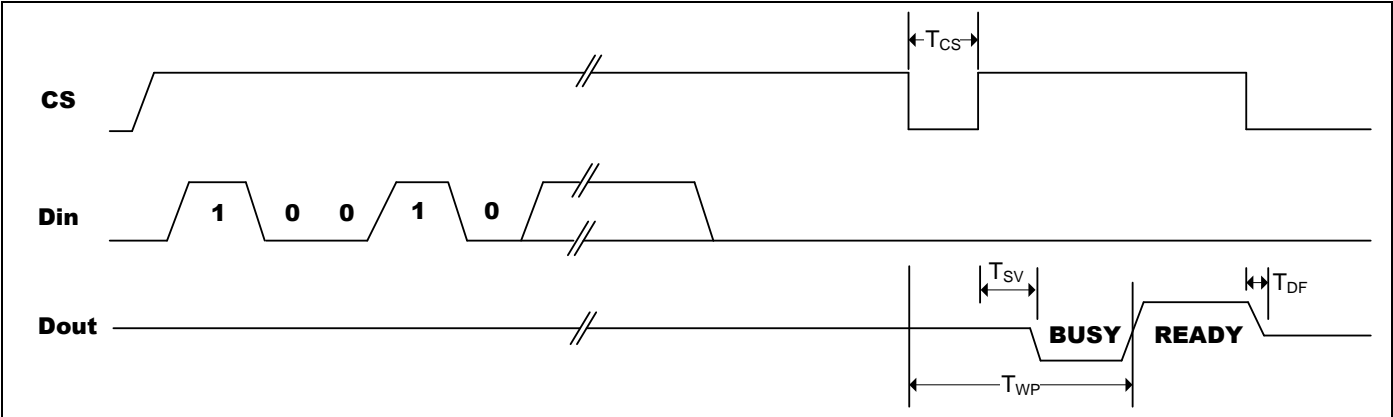[2] To determine data bits An - A0, see Instruction Set for the appropriate device.

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6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to V_{CC} + 1	V
V_P	Voltage on Any Pin	−0.5 to V_{CC} + 1	V
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive Grade 2	−40°C to +105°C	2.5V to 5.5V

6.3 Reliability

Ambient Temperature (TA)	Symbol	Parameter	Min.	Unit
Ta=+25°C	End	Endurance	1 million	Program / Erase Cycles
	DR	Data Retention	100	Years

6.4 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

6.5 Power Up/Down and Voltage Drop

/CS must track VCC during
VCC Ramp Up/Down

Vcc

/CS

Time

Vcc

Vcc(max)

Chip Selection is not allowed

Vcc(min)

T_{wait}

Instruction
Allowed

T_{fall}

T_{rise}

V_{bot}

T_{poff}

Time

Power down-up Timing
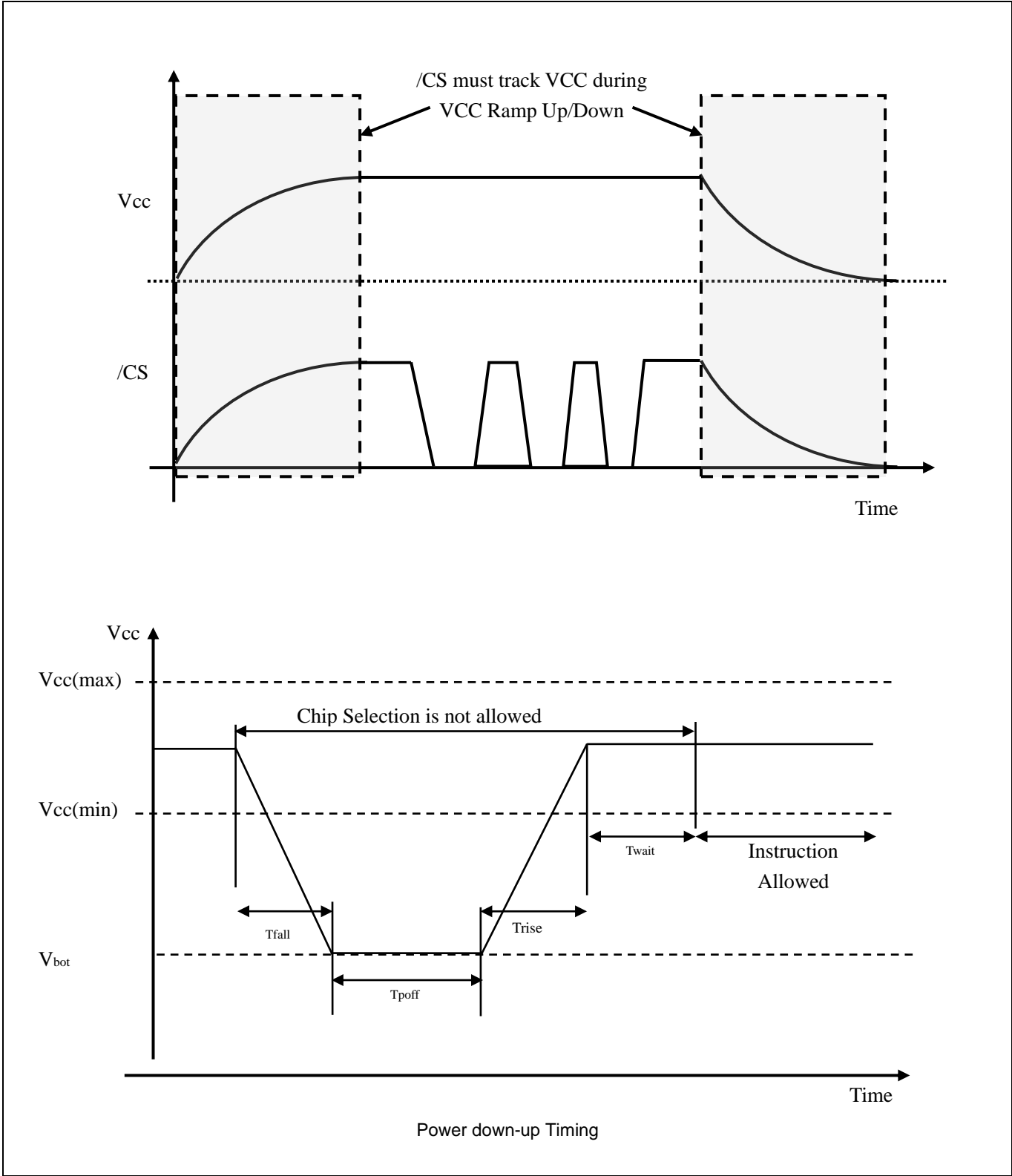
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Symbol	Parameter	min	max	unit
V_{bot}	VCC at power off		0.2	V
Tfall	VCC min to Vbot	1		ms
Tpoff	VCC at power off time	20		ms
Trise	Vbot to VCC min		1	ms
Twait	VCC Min to Instruction	2		ms

* All parameters may be changed after the design or process change.

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6.6 DC Electrical Characteristic

Automotive: T_A = −40˚C to +105˚C, V_{CC} = 2.5V ~ 5.5V

Symbol	Parameter[1]	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		2.5	5.5	V
V_{OL}	Output LOW Voltage	V_{CC} = 2.5V~5.5V, I_{OL} = 2.1 mA	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = 2.5V~5.5V, I_{OH} = -0.4mA	0.8*V_{CC}	—	V
V_{IH}	Input HIGH Voltage	2.5V to 5.5V	2	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage	2.5V to 5.5V	-0.3	0.8	V
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC} (CS, SK, D_{IN}, ORG)	0	2.5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, CS = 0V	0	2.5	µA

Power Supply Characteristics

Automotive: T_A = −40˚C to +105˚C, V_{CC} = 2.5V ~ 5.5V

Symbol	Parameter [1]	V_{CC}	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			2.5		5.5	V
I_{SB1}	Standby current	2.5	CS = GND, SK = GND, ORG = V_{CC} or Floating (x16), D_{IN} = V_{CC} or GND	—	0.3	1	µA
		5.5		—	0.5	1	µA
I_{SB2}	Standby current	2.5	CS = GND, SK = GND, ORG = GND (x8), D_{IN} = V_{CC} or GND	—	6	10	µA
		5.5		—	10	15	µA
$I_{CC-Read}$	Read current	2.5	CS = V_{IH}, SK = 2 MHz	—	—	0.5	mA
		5.5	CS = V_{IH}, SK = 3 MHz	—	—	1	mA
$I_{CC-Write}$	Write current	2.5	CS = V_{IH}, SK = 2 MHz	—	—	1	mA
		5.5	CS = V_{IH}, SK = 3 MHz	—	—	2	mA

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6.7 AC Electrical Characteristic

Automotive: $T_A = -40°C$ to $+105°C$, Supply voltage = 2.5V to 5.5V

Symbol	Parameter [1] [2]	2.5V≤V$_{CC}$<4.5V		4.5V≤V$_{CC}$≤5.5V		Unit
		Min.	Max.	Min.	Max.	
F$_{SCK}$	SCK Clock Frequency	0	2	0	3	MHz
T$_R$	Input Rise Time	—	10	—	10	ns
T$_F$	Input Fall Time	—	10	—	10	ns
T$_{SKH}$	SK High Time	200	—	200	—	ns
T$_{SKL}$	SK Low Time	200	—	100	—	ns
T$_{CS}$	Minimum CS LOW Time	200	—	200	—	ns
T$_{CSS}$	CS Setup Time	100	—	50	—	ns
T$_{CSH}$	CS Hold Time	0	—	0	—	ns
T$_{DIS}$	D$_{IN}$ Setup Time	50	—	50	—	ns
T$_{DIH}$	D$_{IN}$ Hold Time	50	—	50	—	ns
T$_{PD1}$	Output Delay to "1"	—	200	—	100	ns
T$_{PD0}$	Output Delay to "0"	—	200	—	100	ns
T$_{SV}$	CS to Status Valid	—	200	—	200	ns
T$_{DF}$	CS to D$_{OUT}$ in 3-state	—	100	—	100	ns
T$_{WP}$	Write Cycle Time	—	5	—	5	ms

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

C_L = 100 pF

Input pulse voltages: Per V$_{IL}$ and V$_{IH}$ spec

Input rise and fall times: ≤ 10 ns

Timing reference voltages: half V$_{CC}$ level

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7. Ordering Information

Automotive Grade: -40°C to +105°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
2.5V to 5.5V	GT93C66A-3GLA2-TR	150-mil SOIC
	GT93C66A-3ZLA2-TR	3 x 4.4 mm TSSOP

*

1. Contact Giantec Sales Representatives for availability and other package information.

2. The listed part numbers are packed in tape and reel "-TR" (4K per reel). UDFN is 5K per reel.

3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.

8. Top Markings

8.1 SOIC Package

G: Giantec Logo

366A3GLA2:   GT93C66A-3GLA2-TR

YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package

GT: Giantec Logo

366A3ZLA2:   GT93C66A-3ZLA2-TR

YWW: Date Code, Y=year, WW=week

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:

1. Controlling Dimension:MM

2. Dimension D and E1 do not include Mold protrusion

3. Dimension b does not include dambar protrusion/intrusion.

4. Refer to Jedec standard MS-012

5. Drawing is not to scale

9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline

Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

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10. Revision History

Revision	Date	Descriptions
A0	Nov. 2015	Initial version
A1	May. 2022	Update Logo and other